Study and Design of Low-Power CMOS Double Edge-Triggered Flip-Flop Circuit

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Abstract

Low-power techniques are essential in modern CMOS VLSI design due to the continuous increase of clock frequency and chip complexity. In many applications, the power consumption of the IC clock system, composed of flip-flops and a clock distribution network, is one of the most power consuming subsystem in a CMOS VLSI circuit. As a consequence, the reduction of flip-flops power consumption is a crucial factor in IC design.

In this paper, a new double edge-triggered flip-flop (DETFF) is presented in which power consumption is reduced. Several metrics are available for analysis of CMOS VLSI circuits, such as power consumption, delay, and power-delay product (PDP). In general, a PDP based metric is appropriate for low power portable systems. This paper compares three previously published DETFFs together with our design for their transistor counts, power consumption, and power-delay product. HSPICE simulation results employing TSMC 180nm CMOS technology indicate the proposed flip-flop can reduce effectively power consumption up to 39.62% and decrease power-delay product up to 76.78% respectively, as compared to other DETFFs.

Keywords: double edge-triggered flip-flop (DETFF), power consumption, power-delay product (PDP), single edge-triggered flip-flop (SETFF).

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低功率 CMOS 雙邊緣觸發正反器的研究與設計

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摘　要

在 CMOS 超大型積體電路設計中，由於時脈頻率和晶片複雜度的持續增加，降低晶片功率損耗是必要的。時脈網路的功率損耗中，正反器所消耗的功率佔時脈網路功率損耗的絕大部分。因此，透過降低正反器的功率損耗達到降低晶片總功率損耗便顯得非常的重要。

本文提出一種新型低功率損耗 CMOS 雙邊緣觸發正反器電路設計。在 CMOS 超大型積體電路設計中，可以透過功率損耗、傳遞延遲和功率延遲乘積(Power-Delay Product; PDP)等參數來加以分析比較。通常，功率延遲乘積適用於低功率損耗可攜式系統。在本文中，使用 TSMC 180nm 的製程技術模擬，並與三篇先前之雙邊緣觸發正反器電路，針對電晶體個數、功率損耗和功率延遲乘積加以分析比較。根據模擬結果顯示，本文所提出之雙邊緣觸發正反器可以顯著地減少功率損耗。

關鍵詞：雙邊緣觸發正反器，低功率損耗，功率延遲乘積，單邊緣觸發正反器。

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1. Introduction

Flip-flops are known and widely used in VLSI integrated circuit (IC) design. Power consumption of very large scale integrated (VLSI) chips is becoming an increasingly critical problem as modern VLSI circuits continue to grow and technologies evolve. In portable systems, very low power consumption is desired in order to increase battery life. To reduce the complexity of circuit design, a large proportion of digital circuits are synchronous circuits; that is, they operate based on a clock signal. Among the more popular synchronous digital circuits are edge-triggered flip-flops. Edge-triggered flip-flops are often used in computational circuits to operate in selected sequences during recurring clock intervals to sample and hold data.

Edge-triggered flip-flop circuits may be classified into two types. The first type latches data either on the rising or the falling edge of the clock cycle is so-called single edge-triggered (SET) flip-flops. The other type is double edge-triggered (DET) flip-flop, which stores data on both the rising edge and falling edge of a clock signal. The main advantage of using DETFF is that it allows one to maintain a constant throughput while operating at only half the clock frequency. There are several DETFFs have been proposed [1]-[16]. However, the implementation of conventional static DETFF needs many transistors and spends too much silicon area to make them an attractive design alternative in VLSI circuits [3], [6], [13].

In [1], Unger presented some DETFFs, although the flip-flops described in his paper are faster compared with some SETFFs, their complex design has made it undesirable. Lu *et al.* [3] presented a DETFF design which has two loops for maintaining charge levels as a static flip-flop that does not depend on the clock period. This design requires 26 transistors for a CMOS implementation. Gago *et. al.* [4] presented a static DET master-slave flip-flop. The design duplicates a SETFF but shares the clock transistors that are common to both latches. These implementations suffer from a larger clock load at the same level of performance as a SETFF. Llopis *et. al.*[5] proposed a circuit implementation of DETFF which is a modified version of the DETFF proposed earlier in [6]. Complementary logic gates are employed here to balance the output rise and fall times of the original DETFF. Blair [7] provided a static DET design and a semi-static DET design. The static DET design is a modified version of Hossain's static design. Strollo *et al.* [8] proposed a single-latch DETFF. Its operation is highly

dependent on the internal clock buffer sizing and the propagation delay of the internal clock buffers. Varma *et al.* [9] provided a static DET design and a dynamic DET design. This includes a 16-transistor CMOS implementation of the static design in which the availability of an inverted clock is assumed. The design requires two more transistors if the clock is to be inverted locally.

Though several contributions have been made to the art of DETFFs, a need evidently occurs for a design that still further improves the relative power consumption of DETFFs. The remainder of this paper is organized as follows. Section II presents a brief description of existing double edge-triggered flip-flops. The proposed DETFF is described in Section III. The simulation results and a comparison between the existing DETFFs and the proposed DETFF in terms of power and delay are discussed in Section IV. Finally, the last section is a conclusion and summary for this paper.

2. Existing double edge-triggered flip-flops

A conventional SETFF is triggered either at the rising edge or the falling edge of a clock cycle. Referring to FIG. 1, it illustrates the circuit structure of a typical conventional rising edge-triggered flip-flop. However, the operation is merely performed at the rising edge of a clock and cannot be performed at the falling edge of the clock. These arrangements are inefficient as half of the clock edges being wasted, data flow tends to be slow.

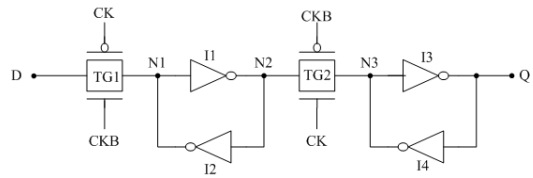

Fig. 1 The conventional SETFF

Several DETFFs have been described by replicating the latch elements of a SETFF and multiplexing the outputs. This paper compares three previously published DETFFs with our proposed design for their transistor counts and power-delay products.

Hossain *et al.* [6] have provided a static DET design which including a 16-transistor CMOS implementation of the static design, arranged in a parallel configuration shown in FIG. 2. The design also comprises two latches, each of which has a loop within itself for maintaining charge levels for providing static functionality. The feedback path in each loop includes an inverter and is switched by the clock. The loops are also isolated from each other. To compare with the SETFF shown in FIG. 1, the circuit only has four more transistors. However, this circuit suffers from sub-threshold currents

due to the threshold voltage drop across the pass transistors. These can be eliminated using full transmission gates; however this raises the number of transistors which switch with the clock signal from 8 to 14.

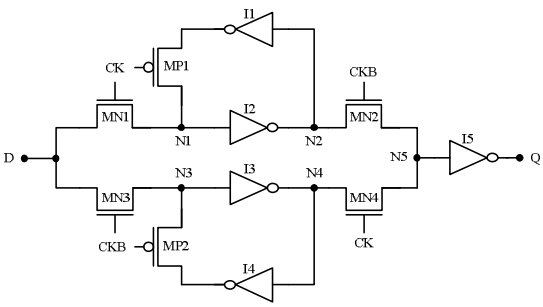

Fig. 2 DETFF reported in Ref. [6].

Kuo *et al.* [10] have proposed a DETFF which employs six switches and four inverters shown in FIG. 3. The switches MN1, MN3, MN5 and the inverter I1 form the upper loop, and the switches MN2, MN4, MN6 and the inverter I3 form the lower loop. These two loops use same feedback inverter I2 and same output inverter I4. This circuit only uses 14 transistors, which is less transistors than in any current double edge-triggered flip-flop construction and which is only has two more transistors than the SETFF shown in FIG.1. According to this circuit, one of these two loops always samples the data and the other loop always holds data. In other words, when the clock pulse changes from low to high, the upper loop holds data and the lower loop samples data, but when the clock pulse changes from high to low, the upper loop switches to sample data and then the lower loop switches to hold the data.

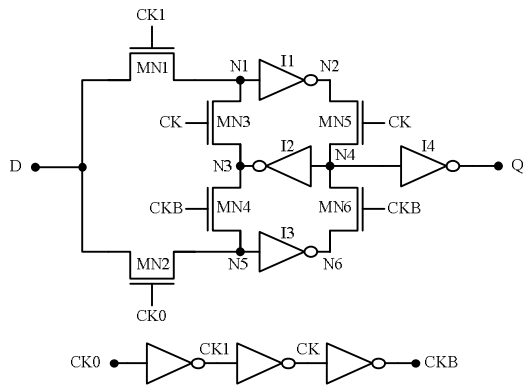

Fig. 3 DETFF reported in Ref. [10].

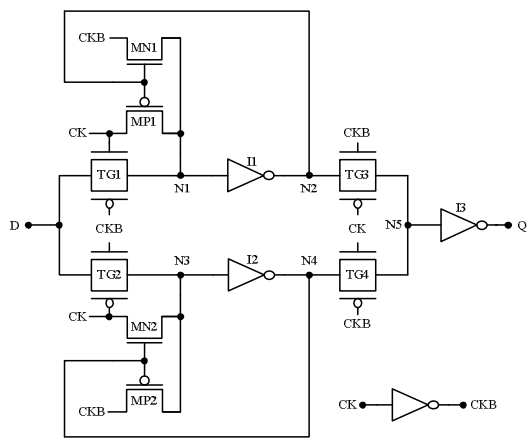

Fig. 4 DETFF reported in Ref. [11]

Pedram *et al.* [11] have proposed a modified version of Hossain's flip-flop (see FIG. 2). In this flip-flop, the role of the clock signal and the data signal is reversed in the feedback transmission gate loops of the storage latches. The main modification is in the feedback portion where the

transmission gate and inverter have been replaced by two transistors, thereby reducing the overall transistor counts as well as the load on the clock signal. The main drawback of this circuit is the use of pass transistors instead of transmission gates, in order to reduce the total transistor counts. This results in reducing the driving capability of the succeeding stages and causing DC power consumption in the output inverter as explained in [12]-[13].

3. Proposed double edge-triggered flip-flop

The proposed DETFF is illustrated in FIG. 5. This design can be thought of as a parallel connection of two latches, one transparent when the clock is logic high and the other transparent when the clock is logic low, with a multiplexor selecting the output of the latch that is in hold state.

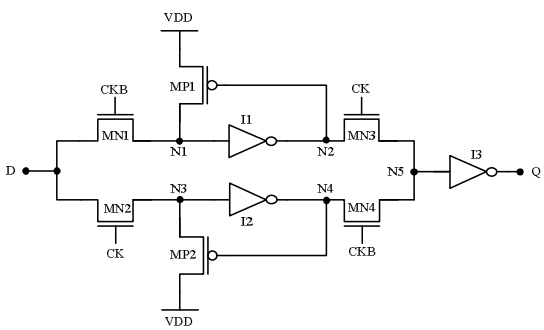

Fig. 5 The proposed DETFF

The feedback PMOS transistors MP1 and MP2 restore the logic high voltage level following the threshold voltage drop of the NMOS pass transistor. In the upper data path, transistor MP1 provides feedback to pull up storage node N1 substantially to a VDD voltage when signal node N2 is logic low. Similarly, in the lower data path, transistor MP2 provides feedback to pull up node N3 to a VDD voltage when the signal node N4 is low.

When the clock is in the logic low state, for the upper data path, the input signal D is quickly conducted into the node N2. If the input signal D is logic high, node N1 goes to the logic high with help from the pull-up transistor MP1. Node N1 remains logic high as long as input signal D is at the high level. Meanwhile, for the lower data path, the previously hold data is quickly pass to the output node Q with help from the transistor MN4. On the contrary, when input signal D is logic high while the clock is in the logic high state, for the lower data path, the input data signal D is quickly conducted into the node N4 and the voltage of node N3 goes to the logic high with help from the pull-up transistor MP2. Node N3 remains high as long as input signal D is at the high level. Meanwhile, for the upper data path, the previously hold data is quickly pass to the output node Q with help from the transistor MN3.

4. Simulation and results

To evaluate performance, different DETFF structures discussed in this paper were designed using a 0.18 um CMOS technology. All simulation parameters are shown in Table 1. The clock frequency is kept at 500 MHz. This clock frequency for DETFFs is equivalent to 1 GHz for SETFFs. The simulated waveform of the proposed DETFF is shown in FIG. 6.

TABLE 1: Simulation Parameters

0.18um CMOS Technology					
MOSFET Model：	BSIM 3	Level 49			
Nominal Conditions：	V_{dd}=1.8V	T=25℃			
	Duty Cycle	Rise time	Fall time	Frequency	Sequence Length
Clock	50%	100ps	100ps	500MHz	N/A
Data	N/A	100ps	100ps	N/A	16

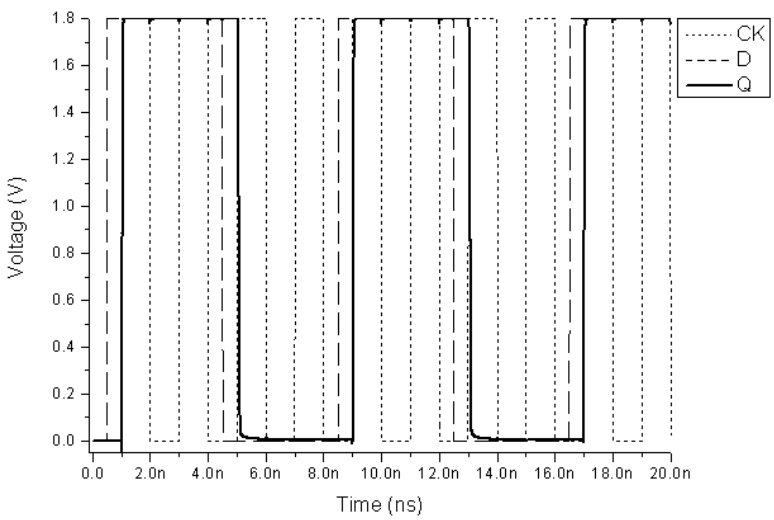

Fig. 6 Transient analysis waveforms of this work

As the power consumption is strongly related to the input data sequence, in the simulations we using the following different data activities: $\alpha = 0$, $\alpha = 0.5$ and $\alpha = 1$ in a period of 128 clock cycles to evaluate the power consumption of these flip-flop structures discussed in this paper. The power measurement of the flip-flops includes the total power dissipated in the flip-flop as well as the local data and clock

power [12]. PDP is calculated as the product of the average D-Q delay and the power consumption for a given data activity. For the edge-triggered flip-flops in Table 2, a comparison among different parameters, only for the data sequence is 11001100 is presented. The parameters include the total number of transistors, the delay from data to the output (D-Q), the total power consumption, and the power-delay product (PDP). Compared with the SETFF shown in Figure 1, as shown in Table 2, the number of transistors in this work is only two more transistors and is less than the other DETFF structures. Furthermore, compared to SETFF, the power consumption of this work is 12.84% less while the power-delay product of this work is 71.37% less, respectively. Most significantly, compared with other DETFF circuits, the presented circuit can save power consumption in the range between 22.80% and 39.62%, and power-delay product (PDP) decreases in the range between 25.63% and 76.78%.

From Table 3, one finds that the proposed circuit always consumes less power than the previously reported DETFFs under different data activities. For the proposed circuit, the saving power percentage is between 38.21% and 51.53% for input data sequence 00000000, between 27.70% and 57.53% for input data sequence 11111111, between 22.80% and 39.62% for input data sequence 11001100, and between 18.87% and 33.26% for input data sequence 10101010, respectively.

TABLE 2: Comparison for data sequence is 11001100 ($\alpha = 0.5$)

FF	# of transistors	D-Q (pS)	Power (uW)	PDP (fJ)
Fig. 1	10	487	42.04	20.47
Fig. 2	16	166	47.46	7.88
Fig. 3	14	416	60.68	25.24
Fig. 4	16	254	56.27	14.29
Fig. 5	12	160	36.64	5.86

TABLE 3: Power consumption of various structures at different data activities

FF	$\alpha = 0$		$\alpha = 0.5$	$\alpha = 1$
	00000000	11111111		
Fig. 1	13.76	11.72	42.04	69.23
Fig. 2	20.83	17.51	47.46	70.70
Fig. 3	25.15	29.81	60.68	85.94
Fig. 4	26.55	25.61	56.27	80.56
Fig. 5	12.87	12.66	36.64	57.36

Figure 7 is the simulation results curve for Table 3. From Fig. 7, one finds that the Pedram *et al.*'s flip-flop consumes more power than the circuit of the other flip-flops by influence of charge sharing. And, the proposed circuit demonstrates the least power-delay product and the least power-delay product under different data sequence.

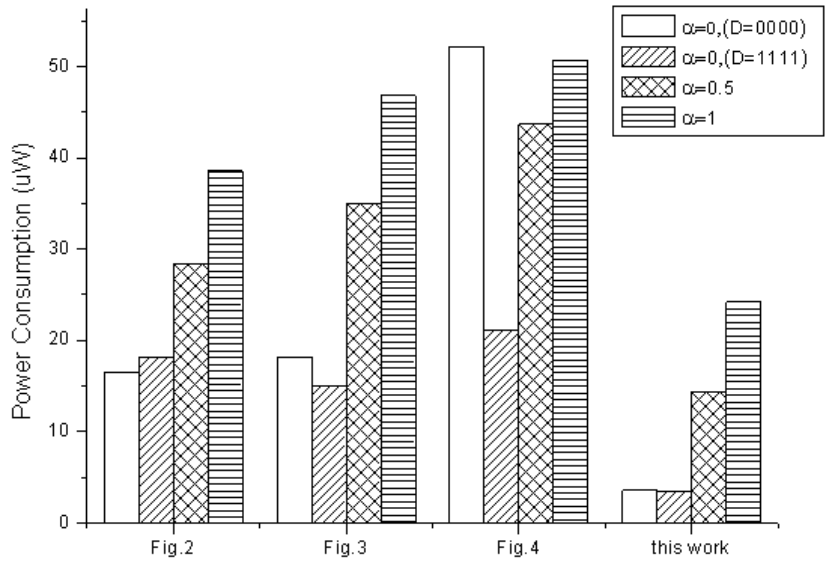

Fig. 7 Simulation results in different DETFFs

5. Conclusion

In the research of low power VLSI circuits, the design of DETFF has gained more attention. The main advantage of using DETFF is that it allows one to maintain a constant throughput while operating at only half the clock frequency. For each DETFF, the average delay, power consumption, and power-delay product are determined as the primary figures of merit. This paper compares three previously published DETFFs together with our design for their delay, power consumption, and power-delay products. The proposed design demonstrates the least power consumption and the least power-delay product under different data sequence.

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