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A Powerful and Sensitive Gauge for Plasma-Process-Induced Damage in Differential Amplifier Circuit Design

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ABSTRACT

Plasma-process-induced damage (PPID) in the semiconductor process is a common phenomenon influencing gate-oxide reliability and circuit performance. How to reduce this effect to an acceptable level is a key issue in recent semiconductor manufacturing. In this paper, a differential amplifier circuit plus designed antenna test patterns to powerfully detect this plasma impact on gate-oxide integrity is proposed. In circuit simulation, the degree of the charging effect in the process from a different back-end metal or via layers on gate-oxide reliability can be effectively gauged. This valuable information can be returned to the process engineers to optimally adjust the plasma process if certain circuit products request a precise and excellent device performance.

***Key Words*: ** plasma process, damage, oxide, reliability, antenna, differential amplifier

差動放大器線路作為電漿製程中一種強有力的感測量具

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摘 要

在半導體製程中，電漿製程對閘級氧化層所造成損傷，是一種普遍的現象。如何降低此效應至可接受的範圍，是現今半導體量產中，一個很重要的議題。在這篇論文中，我們提出一個功能強又靈敏的感測量具 --- 差動放大器線路與天線圖形設計。藉著模擬的結果，可以有效地偵測閘級氧化層的品質，由於後段電漿製程時，所造成的劣化現象，使得氧化層的可靠性變差，進而影響 IC 產品的效益。此珍貴資料，亦可回饋至製程部門，以利電漿製程參數調整，提高量產品質。

關鍵詞：電漿製程，損傷，氧化層，可靠度，天線，差動放大器

I. INTRODUCTION

In the new process technology era, the plasma process as a dry cleaning or etching function is popularly adopted. This process has several advantages [6], especially in etching profile controllability and *in-situ* integration for single wafer processing. However, as the wafer(s) is in the plasma chamber, the charging particles usually depict the non-uniformity behavior. When the charging amount is large enough, the excess Fowler-Nordhein (FN) current can directly damage gate oxide. Furthermore, if the plasma process is at the back-end process such as metal layer or via formation, the charging carriers can also damage the gate oxide through metal line(s) and vias to this connected gate oxide. Then, the oxide integrity will be decayed. The gate oxide will possibly show big leakage or own tremendous traps to decrease the metal-oxide-silicon (MOS) transistor performance such as threshold voltage (V_t) shift.

To avoid or reduce this damage effect, the plasma engineers always adjust the equipment parameters or wafer orientation such as plasma power, etching time, pressure, chemistry, etc. Therefore, the adequate gauge to justify the optimal plasma process is very important. In the past, the charge-to-breakdown (QBD) test [4, 9], the ramping voltage breakdown test, the time-dependent dielectric breakdown (TDDB) test [8, 10], or the hot carrier test [3] to measure gate oxide integrity [5] was popularly applied. However, even the test result of damaged oxide still passes some specified reliability specifications, it doesn't mean that there is no impact for all of circuits. Therefore, verifying this point and investigating the influence of this latent defect in some circuit performance are relatively impressed.

In this paper, for the first time, we demonstrate a differential amplifier circuit [4] plus antenna test patterns as a plasmas gauge. This differential amplifier circuit is not only powerful in plasma sense, but also applied to the real circuit design concern. Here, we will introduce the influence of designed antenna test patterns in plasma process and the simulation results to investigate this degradation phenomenon of gate oxide to impact the circuit performance. The simulation device models are employed with TSMC 0.35um CMOS process technology.

II. WORKING THEOREM

In MOS transistors, the V_t plays a key role in device operation performance. The relationship among V_t, fixed charge, and substrate bias is well-known [12]. For instance, we consider the NMOS transistor.

$$V_t \propto [2\varepsilon_s\, q\, N_a\, (2\phi_F - V_{sub})]^{1/2}/C_{ox} - Q_{fc}/C_{ox} \qquad (1)$$

where ϕ_F: surface potential, ε_s: dielectric electrical constant of silicon, N_a: acceptor concentration in silicon substrate, V_{sub}: substrate voltage, C_{ox}: gate oxide capacitance, and Q_{fc}: fixed charged density of gate oxide.

As the fixed charges are increased owing to plasma process, the V_t value will be fluctuated. Basically, the total V_t shift tolerance below 15% can be accepted in device design. This shift needs cover the gate length variation due to implant, etching, or lithography biases, etc. Therefore, the ratio of V_t shift in the total variation amount due to plasma effect needs to be reduced as small as possible. In general experiment, the V_t values of both NMOS and PMOS transistors are usually measured. From the flat band shift in device, we can justify the electrical polarity of the fixed charges. This information can tell the plasma engineers to choose the adequate plasma parameter(s) to obtain the good etching or cleaning performance and the damage to be the smallest in device performance impact.

From equation (1), V_t depends on Q_{fc} and V_{sub} parameters. Therefore, if the fixed charge amount is changed, we can use the substrate bias to compensate this deviation to the normal device operation. In other words, using this concept in this simulation, we can adjust the substrate bias to replace the charge resources in gate oxide from plasma process. Applying this principle, we can compare the output results of the reference differential amplifier circuit with V_{sub1}=0 and the experimental differential amplifier circuit with V_{sub1}≠0 volt and extract the V_t influence from back bias, seen in Fig. 1.

For differential amplifier circuit operation, first of all, the common-mode operation (i.e. DC amplification) is obtained in simulation procedure because we tune DC V_{in1}, V_{in2}, and V_b to

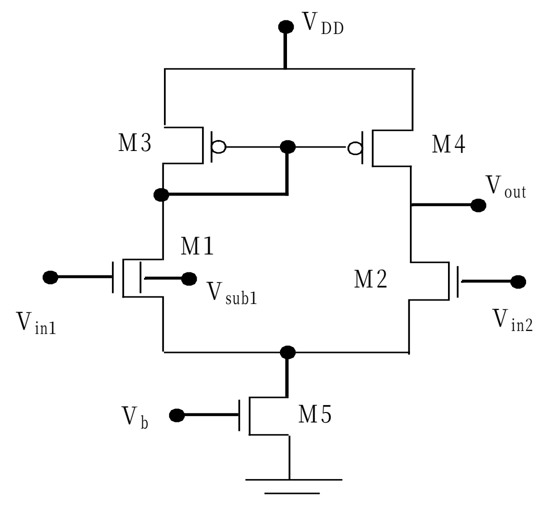


Fig. 1. Schematic of differential amplifier circuit with PMOS load in differential-mode operation

an adequate balance in a normal circuit operation. Then, the AC signals at V_{in1}, V_{in2} terminals are added to examine this fixed charge effect. In transistor selection, M1~M5, we adopt the small channel width and the minimum channel length, W/L, due to the antenna effect concern. However, we also need eliminate the narrow-width device effect due to the fluctuation of lithography or etching process steps.

In the first reference differential amplifier circuit operation, V_{in1} and V_{in2} have equal and opposite signals. M1 and M2 transistors show the equal impedances. When the V_{in1}=V_{in1} + δs, the V_{out} will generate the phase change because of this external δs disturbance. Similarly, if this disturbance is substituted by the internal source, the behavior is still happened. As we apply the substrate bias, $V_{sub1}\neq 0$, to M1 transistor, this transistor gains the extra charge ~ $[2\varepsilon_s qN_a]^{1/2}[\ |V_{sub1}|\ ]^{1/2}$. In other words, this charge amount can be attributed to that from fixed charge to influence the V_t performance. Furthermore, the M1 impedance is slightly changed due to this effect. Therefore, in simulation, we observe while the V_{sub1} is somewhat tuned (~2nV), the V_{out} tremendously has the phase shift.

For an experimental differential amplifier circuit with antenna test pattern, shown in Fig. 2, M1 transistor gains some charging carriers from “designed test pattern” in plasma process. Of course, if the plasma damage is very serious, the gate oxide is dead. This phenomenon can be first detected in wafer-accepted test (WAT) and the wafers will be screened out. Here, we investigate the minor damage to gate oxide integrity and try to quantize the charge amount in circuit impact.

Through the V_{sub1} adjustment to the designed threshold voltage , we can detect the charge absorption in M1 with Eq. (1). In the beginning, this fixed charge in gate oxide would induce the phase change comparing with that in the reference differential amplifier circuit. We tune V_{sub1}, in Fig. 2, and get the same phase with that in the reference differential amplifier circuit. Using this data, we can calculate the amount of fixed charges and the influence of threshold voltage in M1. Furthermore, if we would like to investigate the other polarity of fixed charges more, we may exchange M1 to M3 and M2 to M4. M5 is substituted by PMOS type. The following operation procedures are similar to the previous.

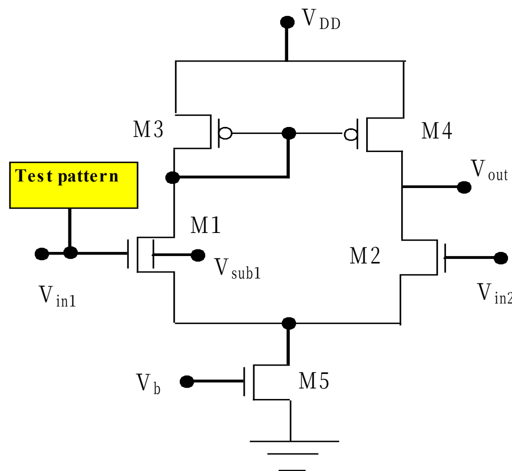


Fig.2. Schematic of differential amplifier circuit with antenna test patterns

III. ANTENNA EFFECT AND ANTENNA PATTERNS

In plasmas process, there is an antenna effect. It means that the charging carriers in reactor will be cumulated to gate oxide of processed wafers such as the effect of wireless telecommunication to receive the signal through an antenna line to the receiver. In the semiconductor industry, there are some antenna rules to clarify the serious degree of antenna effect [13] and constrain the design of metal line routing. If the antenna ratios are higher, the length allowance of metal line is longer or the via numbers are larger. It will be helpful in circuit design without adding a protection diode [7] connected to the gate electrode. In other words, the gate-oxide integrity is strong enough.

For the plasma process improvement, the circuit pattern layout also plays a main role. Actually, the device gate oxide area is larger or the oxide thickness is thicker, then the degree of the plasma-induced damage should be smaller. However, the process technology is requested to be scaling-down in the competing semiconductor industry. The big device gate area or the thick gate oxide can’t be satisfied in circuit design. How to manufacture the robust quality of device gate oxide becomes a huge challenge in the novel process technology.

Some of common specified antenna patterns are depicted in Fig. 3. Each test pattern has its special purpose in the plasma process monitor. For instance, the finger or comb type is to cardinally monitor the edge effect in plasma etching. The space variations of each metal line also illustrate the different behaviors in plasma etching, such as electron shadow monitor with shaded type. The area type is to monitor the photoresist strip and the serpentine is to reflect the longer metal line effect. Again, the influence of the antenna effect from each metal layer with cross-section profile of a NMOSFET is also introduced, seen in Fig. 4.

In Fig. 4, we find the most of plasma charges in this NMOS transistor come from the metal 2 plasma process.

Using these specified patterns, we can distinguish the antenna resource whether it comes from metal line or via. We also can recognize which metal layer has the biggest impact in

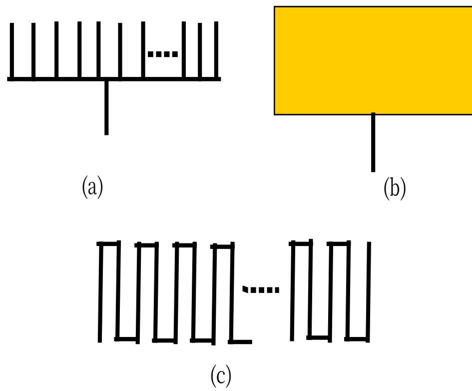


Fig. 3. Simple schematic antenna patterns are demonstrated, (a) finger type with dense, sparse, or shaded shape [2], (b) area type, (c) serpentine type

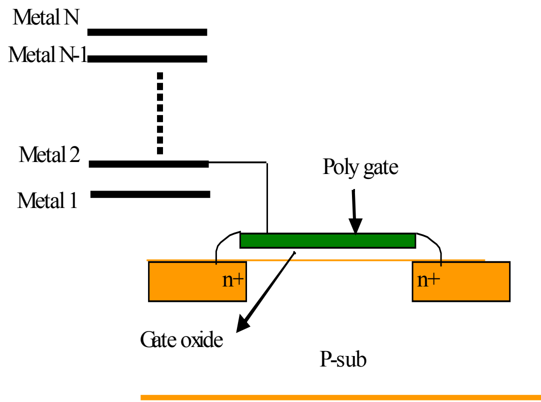


Fig. 4. Cross-section of a NMOS transistor with N-layer metal lines is shown

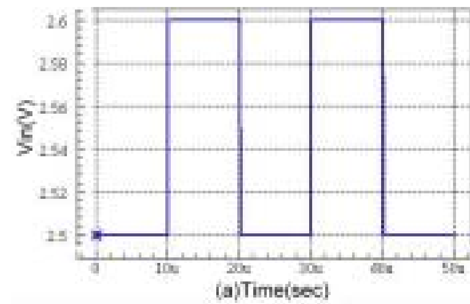
oxide quality degradation. It's a useful and helpful concept. Therefore, this idea was patented in R.O.C. [1] and USA [14].

IV. SIMULATION RESULTS

With 0.35um device models coming from Taiwan Semiconductor Manufacturing Corporation (TSMC), the previous concept is verified.

Fig. 5(a) shows the signal performance of input terminal at the reference differential amplifier circuit. The DC bias is added at this node. The period of the AC signal is, for example, 20u sec. Fig. 5(b) is the output performance. The phase difference between them is 180°. For the experimental differential amplifier circuit replacing with $V_{sub1} \neq 0$, we obtain Fig. 6(a) is the same as Fig. 5(a) as an input signal and Fig. 6(b) exposes the same phase with the result of Fig. 5(a).

According to TSMC's device parameters, we calculate them and obtain the V_{sub1} ~ 2nV is equal to the fixed charge amount, 6.33×10^{-12} C/cm^2. It means that the fixed charge number in gate oxide is ~3.96×10^{7} /cm^2. Due to this impact from plasma damage, the V_t shift is around 14μV, seen in Table 1.



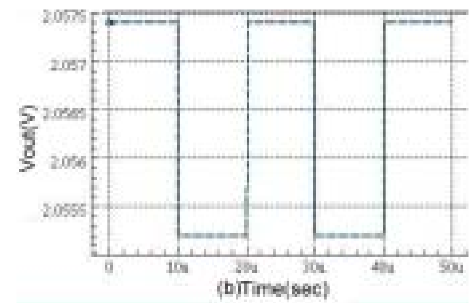
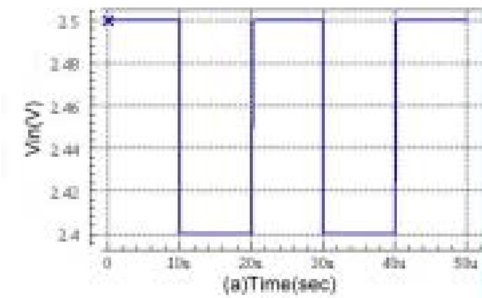


Fig. 5. The signal behaviors of input and output terminals for reference differential amplifier circuit with a signal period, 20μsec, are shown as V_{sub1} = 0V. (a) input signal, (b) output signal



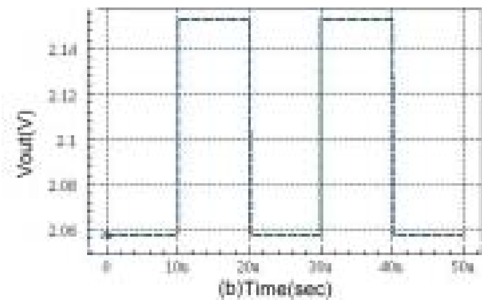


Fig. 6. As $V_{sub1} \neq$ 0V, the phase of the output signal is changed to the identical orientation with the input node. (a) input signal, (b) output signal

Table 1. The simulated fixed charge amount and Vt shift are listed due to substrate bias change

Variable	Value
ΔV_{sub1}	2 nV
ΔQ_{fc}	6.33×10^{-12} C/cm^2
ΔV_t	14 μV

V. CONCLUSION

A powerful and sensitive gauge with differential amplifier circuit in plasma process is demonstrated with TSMC 0.35um CMOS process technology. Through the back bias in silicon substrate, we can summarize that these charges come from the plasma process and are trapped in gate oxide. We have observed one phenomenon. Even the fixed charge amount is small, it will impact some sensitive circuit, like differential amplifier circuit if M1 and M2 transistors are asymmetric. This information is precious for analog or mixed-mode circuit design and process manufacturing to do the compromise between the circuit accuracy and the process controllability. Of course, the adequate antenna test patterns in plasma monitor are also remarkable as a good assistant.

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