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A Powerful Electrical Probing Method to Detect the Kink Effect of MOSFET Devices

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ABSTRACT

In a submicron or deep submicron process era, the integrity of metal-oxide-semiconductor field-effect transistor (MOSFET) is more and more strictly requested. As the generic process development is launched or the mass- production line has some variation, the gate oxide quality under gate electrode is sometimes uncontrolled. Therefore, the device characteristics depict abnormal behaviors such as the kink effect. How to detect this phenomenon and analyze the failure distribution in a wafer or in a wafer lot is a big issue. Here, a method of testing a transistor with second derivative of a numerical method as an electrical prober is proposed. Furthermore, this testing algorithm can be effectively implemented into an auto testing program to probe whether the tested MOSFET transistors have the hump situation. Then, the researchers or the process engineers can utilize this useful information to seek some solutions to overcome that. This test method shows that it is a helpful assistant in monitoring a quality device.

Key Words**:** integrity, gate oxide, kink effect, auto testing

一種強有力的電子量測法以偵測場效電晶體元件的捲縮效應

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摘 要

在次微米或深次微米的製程中，場效電晶體的品質要求是愈來愈嚴格。當新製程開發在試產時或量產線上有製程變動時，閘極的氧化層常有品質控制不佳的現象。因而，造成元件特性曲線有不正常的行爲表現，諸如捲縮效應等。如何偵測此現象，並分析元件故障分佈於一晶片或一整批晶片中，實是個棘手的問題。在這裡，我們提出一種藉著二次微分的數值分析電性量測法，以檢測元件的優劣。接著進一步，將此測試流程有效地轉成自動量測系統。一方面，可大量地量測，以判別各種場效電晶體元件良窳；另一方面，可得統計的資料，以利製程改善。

縮短製程技術開發時間或加快產品量產速度。

關鍵詞：品質，氧化層，捲縮效應，自動量測

I. INTRODUCTION

As the characteristic of a MOSFET device has some variation due to the oxide thinning localized at the side of gate isolation region, this phenomenon can't be quickly detected in production line. Usually, the engineers observe this device behavior by hand and obtain the limited data. Some of destructive test methods [2, 3, 5-7] are employed. However, they will delay the process development time and sometimes mistake the root cause with the little data. How to collect the tremendous data and investigate them with statistics is an urgent task.

In this paper, for the first time, we demonstrate a non-destructive method of testing a transistor with a second-derivative way [8]. Owing to the development of this algorithm, the kink effect [1, 4] in MOSFET devices can be immediately sensed in auto test, called wafer accepted test (WAT). The degradation of this effect also may be quantified. Of course, the huge data can be cumulated through the enough tested wafers. Because of the large information showing the distribution of failure devices, the accurate solution can be effectively and accurately searched.

In other words, the process development time can't be retarded. Time-to-market can be approached soon.

II. WORKING THEOREM

For a normal MOS transistor, the electrical curve of the source/drain current, Ids, versus the gate voltage, Vg, is smoothly bended from the triode region into the saturation region. On the contrary, if the electrical curve is abnormal, we can derive the operation function of this transistor is twisted. For some serious case, this kind of transistors will strongly influence the circuit performance. In order to improve that, some of process steps should be optimally tuned to the requested device performance. In a I-V curve, I(V), if there is a hump situation, it means that a turning-point range will be generated in this curve. We can treat this hump phenomenon as the superposition of two curves. Hence, as this hump curve is derived by twice, called g(v), the turning-point effect will be exposed in this new curve.

$$g(V)=\frac{d^2I(V)}{dV^2} \qquad (1)$$

where g(V) is the representative of the second derivative of I(V) curve.

Actually, for a normal Ids vs. Vg curve, even the second derivative is applied, the final derivative result, where the Vg is employed in the triode region or more, shows the smooth curve and the derivative data result is less than zero. However, the hump curve obviously depicts the peak and valley results. The worse hump, the higher peak value.

According to the magnitude of the peak value or the difference between the peak and the valley at curve g(V), we can figure out the serious degree of the kink effect and return this information to the process development or the production line related persons to seek the suitable solution(s).

III. TEST RESULTS

While the process precision is requested more such as under half micron range, the kink effect in some MOSFET devices is frequently observed. The normal and abnormal curves of source/drain current, Ids, versus gate voltage, Vg, were obtained in Fig. 1. The curve A and the curve B represent the normal device and the abnormal device, respectively. Furthermore, the dotted circle range, in Fig. 1, indicates the hump location. These I-V curves were originally sensed with HP4156C semiconductor parameter measurement instrument. The following MOSFET transistors attribute to N-channels.

After the second derivative with the gate voltage variable for the normal and abnormal I-V curves, we inspect that there exists a hump phenomenon in the abnormal curve as gate voltage > threshold voltage, Vth with the measurement metrology of the maximum transconductance measurement,

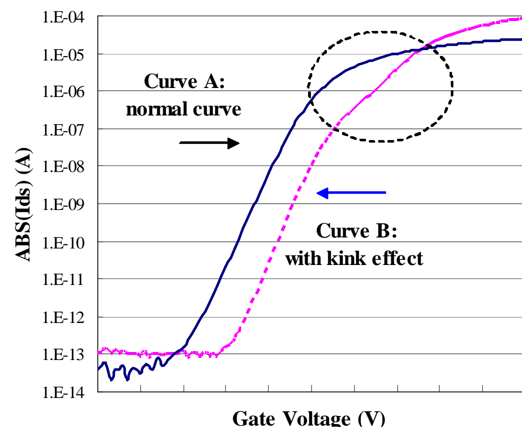

Fig. 1. The characteristics of source/drain current, Ids, versus gate voltage at wafer edge are exhibited

seen in Fig. 2. The abnormal curve shows the peak-and-valley points as the applied gate voltage is greater than Vth. The normal curve without the turning point in the triode region of this MOSFET transistor is observed. The magnitude of the kink effect can be defined as the subtraction value between Ids2max1 and Ids2min2 or the Ids2max1 value, which is greater than zero, in Fig. 2 as a justification factor. Here, Ids2min1 means the first minimum Ids value in second derivative. Ids2max1 indicates the first maximum Ids value in second derivative. The final Ids2min2 illustrates the second minimum Ids value in second derivative.

Observing the second-derivative result of the normal curve in Fig. 2, we find that as the gate voltage is far from the threshold voltage, the curve only shows a minimum valley point. The g(V) values of measured points at the right hand side of this minimum valley point are under zero.

Fig. 3 shows the characteristic of a bad device at the central site of wafer. After the second derivative in Fig. 3, we obtain the behavior in Fig. 4 similar to that in Fig. 2. We employ the schematic diagrams, in Fig. 5-7, to illustrate the locations of the bad devices. Sometimes, they exist at the edge sites of wafer, but they occasionally show at the central sites of wafer. Of course, if the worst case is happened, all of bad devices will be observed at the full wafer. The “X” symbol, in Fig. 5, means that there is a hump in this tested MOSFET device. Through these figures, they illustrate the kink effect of MOSFET devices strongly depends on the side of wafers. It means that the location of gate oxide growth in a wafer, attributing the impact of gas flow, furnace temperature distribution, or surface roughness, etc., cardinally influences the MOSFET performance.

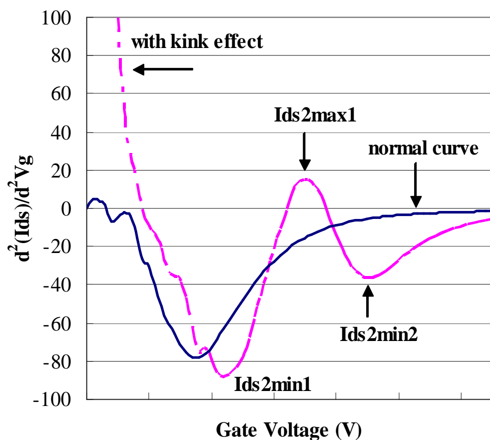

Fig. 2. The normal and abnormal I-V curves are differential by twice

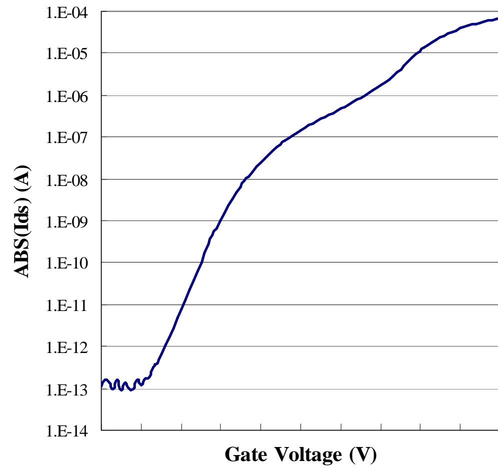

Fig. 3. The kink effect of this abnormal curve at the central site of wafer is measured

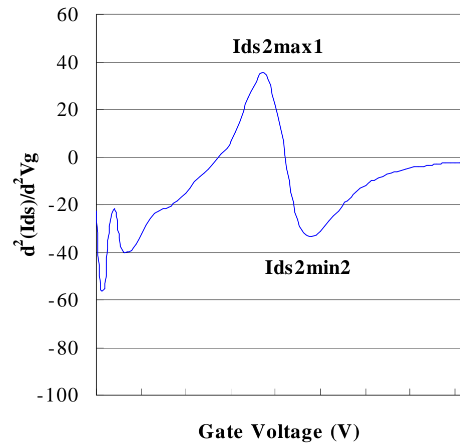

Fig. 4. The derivative curve at the central site shows the bigger different value between Ids2max1 and Ids2min2

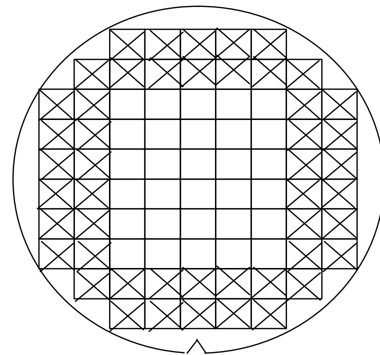

Fig. 5. The kink effect of MOSFET devices is sprinkled at the edge sites of a wafer

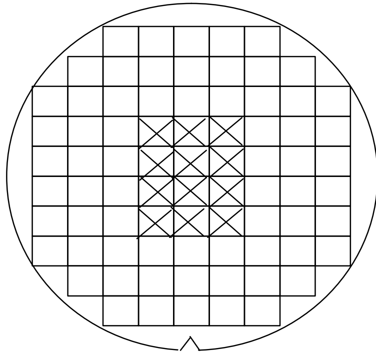

Fig. 6. The distribution of the kink effect of the tested MOSFET devices is localized at the central sites of a wafer

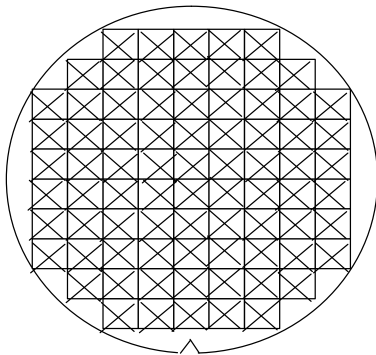

Fig. 7. The kink effect of MOSFET devices covers all of sites in a wafer

In the next test results, a variety of the distributions of the kink effect of the tested MOSFET devices under the different test sites in a wafer are schematically displayed. The test algorithm was implemented into an auto-test program at the auto testers, HP4071 and Keithley S630 at UMC, Taiwan. For the generic process development, people concern the front-end process. Therefore, as the metal 1 process with some passivation layer is completed, engineers will request to test these wafers. For the mass-production line, all of wafers are full-run. 5-die per wafer test is popularly employed.

Combing this test method and the data processing in the auto test, we can fast gain the abnormal wafer(s) in a wafer lot or during a long period of test time. It shows that this test method can be seen as a powerful prober in failed device detection.

IV. DISCUSSIONS

Through the collected data such as Fig. 1, the hump location is, usually, at the triode region or closed to the pinch-off point in I-V characteristic curves. Therefore, as we would like to choose the justification in the test program, we will, first of all, ignore the initial test points. Because these points are not related to the hump detection, we need screen them out to avoid the failure justification.

The kink effect, basically, points out that there are two-device behaviors in a MOSFET transistor. It means that this transistor at some gate voltage is non-uniformly turned on. This situation is, fundamentally, prohibited in circuit operation. By the past process experiment, we obtained that some of the root causes generated from the oxide-thinning-in-Local-oxide (LOCOS) process, seen in Fig. 8-9, owing to forming the bird's beak. The other was such as the shallow-trench- isolation (STI) process to thin the edge oxide at the quarter-micron process or below. Of course, the narrowing electrode gate in the edge or in the center due to the lithography disturbance, etching bias, or particle contamination was also a possible root cause. However, this phenomenon can quickly be inspected with optical microscope or checked with the kink-effect distribution to confirm that.

In Fig. 8, the cut line, cross-section line, through poly gate will illustrate the cross-section profile of this device in the next figure.

The location of LOCOS oxide and gate electrode, in Fig. 9, is also pointed out.

While the thickness of the edge of gate oxide adjacent to the LOCOS in Fig. 9 is, for instance, thinner than that of the center of gate oxide, this MOSFET transistor, in this time, owns two oxide thicknesses and will display a two-device I-V characteristic curve. The transistor will be turned on first due to the thinner-oxide region, but the dominant current comes from the central oxide region. Because the turning time of this device can't follow the original design spec., it will disturb

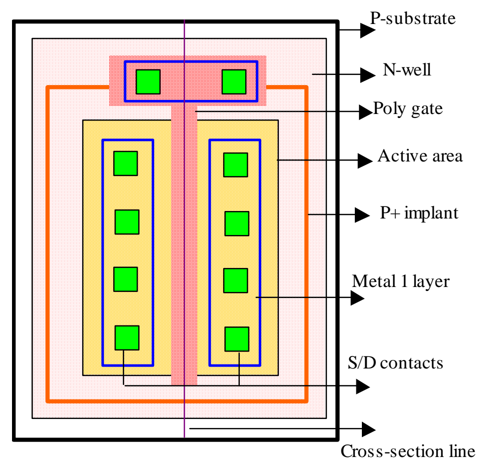

Fig. 8. A schematic of the top view of a PMOS transistor with the definition of each layer is shown

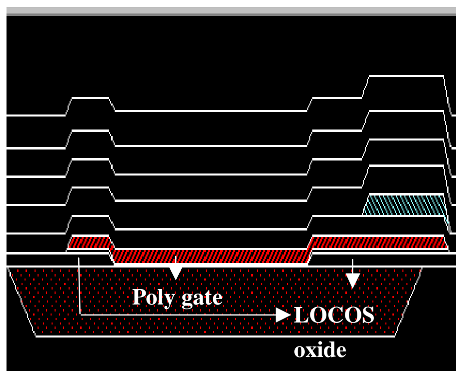

Fig. 9. The cross-section of a PMOS device is depicted

the other next-step transistor operation in the initial design plan. The other phenomenon of this curve at the saturation region in this kink-effect transistor shows the higher saturation Ids. If the Ids is over tolerable design specification too much, the circuit performance will be seriously degraded. Moreover, this kind of products will probably show the function fail and can't be accepted in product delivery.

V. CONCLUSION

A powerful electrical probing method with non-destructive detection of a second derivative way in I-V characteristic curves is investigated and exposed. Through the verification with manual measurement and auto testers at United Microelectronics Corporation (UMC), this testing method is confirmed that it is a powerful tool to extract the abnormal devices during process variation. It is also a good assistant in generic process development to obtain the optimal process condition, especially in LOCOS or STI process combing with gate oxide growth.

With the data analysis through management information system (MIS), the engineers can easily monitor the abnormal wafer(s) with the kink effect in a lot or some lot(s) in a long manufacturing period such as a quarter or half a year. Using this method, some of process development time is shortened and the process deviation impacting the device performance issue can also be adequately controlled well.

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