Electrical Characteristics Analysis with 3-D Simulation on FinFET

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Abstract: A triple gates fin field effect transistor (FinFET) simulation is presented. The theoretical study is focused on the three dimension (3D) device design and simulation of FinFET with different gate length (L_{gate}), FinFET height (H_{fin}), and channel thickness (T_{fin}). Electrical characteristics of deep submicron FinFETs including threshold voltage saturation (V_{Tsat}), drain induced barrier lowing (DIBL), subthreshold swing (SS), and on-to-off current ratio are analyzed. Special emphasis is focused on optimization of device design and suppression of short channel effects (SCEs). It is showed that the device and fabrication technology to be developed in the present work will be successfully applicable to the realization of FinFETs with low DIBL(<50mV/V)、low SS (<90 mV/decade), and high on-to-off current ratio($10^{5.3}$ times) and with T_{fin} of around 2 nm and H_{fin} of around 1.4 nm FinFET would promise a better electrical characteristic.

Keywords: FinFET/鰭形場效電晶體, V_{Tsat}/飽和門檻電壓, short channel effects/短通道效應, drain induced barrier lowing/汲極引發能障降低, subthreshold swing/次臨界導通斜率, on-to-off current ratio/電流開-關比

以三維電腦模擬分析鰭形場效電晶體之電性—陳聰敏

摘要：本研究主要針對鰭形場效電晶體(FinFET)元件設計及三維模擬（3D dimension）。場效電晶體之閘極長度（gate length, Lgate）、高度（H_{fin}）、及通道厚度（channel thickness, T_{fin}）適當之調變，經由 3D 模擬做詳盡之理論分析。深次微米之鰭形場效電晶體其短通道（short channel）引發之各種效應，如飽和門檻電壓、汲極引發能障降低（DIBL）、次臨界導通斜率(SS)、及電流開-關比(on-to-off current ratio)均有詳細之理論分析。本研究所得之結果有助於 FinFETs 之元件設計及製作技術開發，T_{fin} 在 2 nm 左右及 H_{fin} 在 1.4 nm 左右預期可以得到較佳之 DIBL<50mV/V、SS <90 mV/decade、及 on-to-off current ratio $10^{5.3}$倍。

Introduction

As the feature size of vary large scaled integration (VLSI) is scaling down, the influence of gate electrode on channel conductivity decreases significantly. In addition, the punch-through effect becomes much serious, which strongly degrades the device performance. To overcome such issues, some advanced structures, including FinFETs, silicon-on-insulator (SOI) devices with ultra-thin body (UTB), and Schottky barrier (SB) MOS transistors have been proposed [1-5]. The use of FinFET, which is with a free-stand three-direction channel, has been shown being able to enhance the function of gate on channel conductivity control and release the punch-through effect. On the other hand, The FinFETs is a special kind of multi-gate (MG) MOS device that has been shown to be very effective in the suppression of short-channel effects [4-5]. However, the partial inducing capability of channel causes the sensitivity of electrical characteristics. Thus, the FinFET dimensions must be designed for higher on-stat current and lower off-leakage current. Because of FinFET with excellent roll-off characteristics, e.g., the driving current and manufacturability,. this structure makes it possible to overcome the SCEs with a lightly doped or un-doped channel [6]. The feature is advantageous for scaled devices especially of DRAM cells and CMOS devices [7]. However, the SCEs of the FinFET are essentially 3D phenomena that are sensitive to the geometry of the device. Accordingly, 3D process and device simulations are indispensable to design an optimal structure of FinFET [4-10].

The deep submicron FinFETs devices with low drain induced barrier lowering (DIBL), low subthreshold swing (SS), high on-to-off current ratio, low specific on-resistance ($R_{sp,on}$), low power loss(P_D), high switching speed and high driving capability, etc., have been urgently required in electronic ULSI industry [8,12]. Essentially, DIBL, SS, low leakage current and driving capability of FinFETs are key factors in determining the quality of MOSFETs for deep-submicron device applications, which strongly depend on the device geometry size. In general, a larger device structure would result in a lower SCE but a higher device volume, while a smaller device structure shows an inverse situation. How to solve or release the trade-off problem between SCE and device geometry size, how to minimize the DIBL, SS and driving current of FinFET's device, how to improve the switching speed of FinFET's device to approach its theoretical value, and how to minimize the power loss of FinFET without sacrificing other device properties, are still open problems in the FinFET fabrication.

In this work, 3D simulation and design on triple-gate FinFETs is presented. ISETCAD simulator including Devise, NOFFSET, and fully 3D device simulator Dessis were used, which calculates the currents and electric fields in the devices using a Poisson–Schrödinger solving algorithm [13]. Dependence of electrical characteristics and device geometrical parameters such as L_{gate}, T_{fin}, and H_{fin}, etc., were analyzed and discussed. Device simulations predict good performance down to 17 nm gate length. Special emphasis is

focused on the optimization of device design and the impact of SCEs in FinFETs. Guidelines for device design will also be proposed.

Device geometry

Device geometries and dimensional definitions are shown in figure 1. It is noted that there is a triple-gate wrap around the ultra thin un-doped or light-doped (1×10^{16} cm^{-3}) channel, which could enhance the channel conductivity and reducing the leakage current. In general, a larger channel doping would result in a higher DIBL but a lower carrier mobility, while a lower channel doping shows an inverse situation. In this process, triple-gate FinFET can provide improved short-channel behavior suitable for achieving international technology roadmap for semiconductors (ITRS) projections [14]. The structural and geometrical parameters of FinFET used in simulation are as follows: L_{eff}=17~38nm, T_{fin}=5~15nm, H_{fin}=5~15nm, and T_{ox}=1.4~0.9nm. Thus, achieving the desired threshold voltages will be a significant challenge in triple-gate devices. The process described here is for n-channel FinFET simulation. The following describes some critical dimensions of the FinFET structure as Fig.1 shown in this process:

Gate length (L_{eff} and L_{gate}): In this process, the physical gate length of the FinFET is defined by the spacer gap.

Device width (T_{fin}): Because the current flows along the horizontal surfaces of the fin, the width of the FinFET quals the fin width. The width definition only counts one side of the channel, which is the typical definition for trible-gate devices.

Body thickness (H_{fin}): Because there are triple gates controlling three sides of the fin, the fin channel thickness for FinFET devices equals to the fin body thickness.

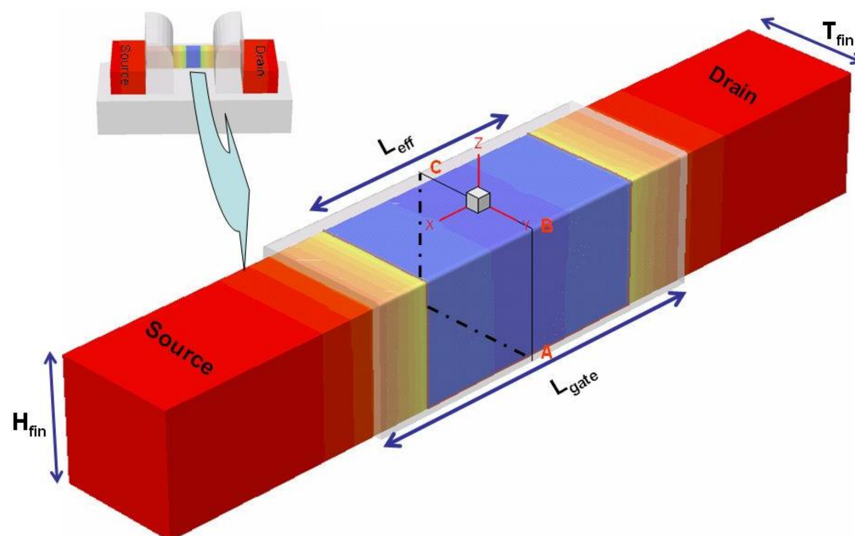

Fig. 1 Schematic and dimensional definitions of the simulated triple-gate FinFET structure.

Results and discussion

The simulation results of the conduction-band energy distributions of triple-gate FinFET transistor near the middle cutting plane of channel volume are presented in Fig. 2. The three variants for triple gate nMOS FinFET shown in the figure differ from each other by different biased voltage. One is the gate biased voltage to be set 0 V (defined as off state). Another is biased at 0.303 V (threshold voltage, V_{Tsat}, based on the simulation results). The other is the gate biased at 0.8 V (on state). The strong variation of conduction band energy is exhibited near the surface of FinFET, in particular, near the corners of FinFET. Based on the same cutting plane, Fig. 3 exhibits the topographic charts of current density distributions for the same three biased conditions. No leakage current enhancement in the corners of the fin is observed. In contrast, a depletion of the leakage current in the inside body of the fin is seen in Fig. 3(a). The depletion is much more pronounced in the triple gate FinFETs. For the V_g=V_{dd} sample of Fig. 3(c), the current density is mainly concentrated close to surface and drops down rapidly. On the other hand, the maximum current density of off state exists beneath the center of the cutting plane and that of on state comes up in the corner region of FinFET. Moreover, the current density concentrates underneath the part of the center as gate biased at V_{Tsat}. This result is similar to the electronic characteristics of the fully depletion MOSFET (FDFET) device. The enhancement of current due to corner effect extends only over a very small region near the corner. This is due to a short screening lengths inside of the inversion layer. The major effect in the triple-gate transistor is the suppression of the current near the upper surface of the fin. The reason is that the gate-inducing capability is strong significantly at the corner and can not be apparent beneath the center of FinFET device.

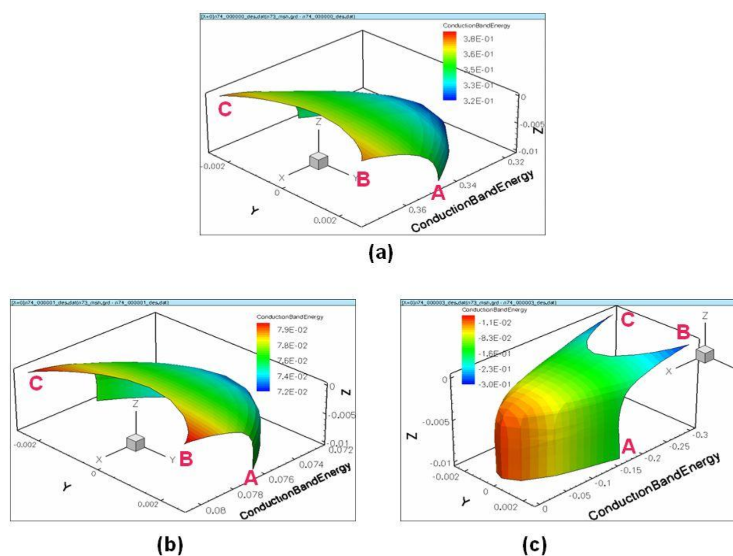

Fig. 2 The topographic charts of conduction-band energy near the middle of channel under the different gate voltages: (a) Vg = 0 V, (b) Vg = 0.303 V, and (c) Vg = 0.8 V.

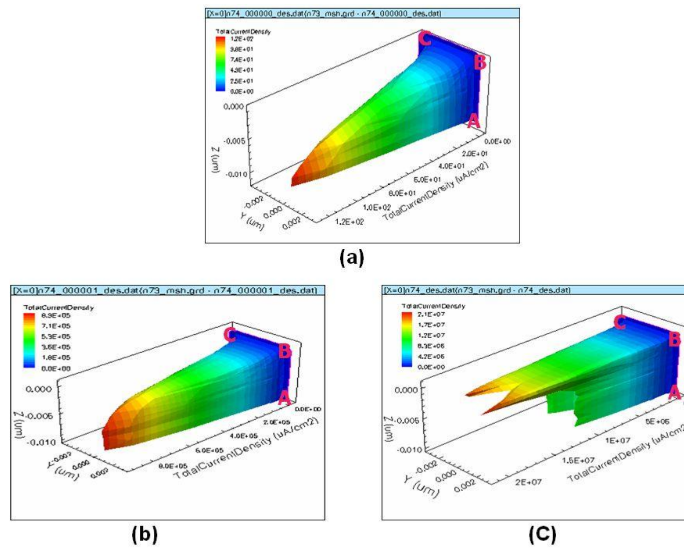

Fig.3 The topographic charts of current density near the middle of channel under the different gate voltages: (a) Vg = 0 V, (b) Vg = 0.303 V, and (c) Vg = 0.8 V.

To further clarify the electronic characteristics of the corner effect of the triple-gate FinFET, we present some of the current density distributions inside of the transistor. Based on the cutting plane (see Fig. 1), the on-state current density distribution near the surface of vertical gate was shown in Fig.4(a). According to the three 1D current density distribution curves, the maximum current density appears at the position, which is 1.4 nm under the corner. Furthermore, the on-state current density distribution near the channel bottom shown in Fig. 4(b). From the three 1D current density distribution curves, it is found that the maximum current density occurs in a region with a distance of about 1 nm to the surface of the channel. According to the calculated results, FinFET with T_{fin} of around 2 nm and H_{fin} of around 1.4 nm would promise a better electrical characteristic.

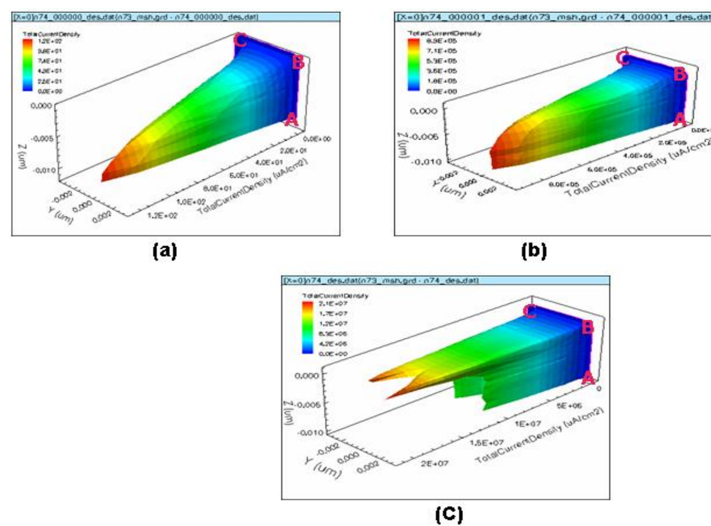

Fig. 4 The on-state current density of the cutting lines: (a) near the middle region of vertical gate surface, (b) near the middle region of the channel bottom.

Fig. 5 and fig. 6 show the V_{Tsat} variations as a function of T_{fin} and H_{fin}: one is the constant L_{gate}, which was considered the T_{fin} and H_{fin} effects, and the other is the constant T_{fin} which was studied the H_{fin} and L_{gate} effects. For reference, the V_{Tsat} profile is also shown. Furthermore, there are confined L_{gate} to 18 nm, 25 nm, and 37 nm, respectively. In these figures, it can be seen that: (1) the V_{Tsat} decreases with the increase of T_{fin}; (2) the V_{Tsat} decreases with the increase of H_{fin}; (3) the V_{Tsat} variations of T_{fin} is more significant than that of H_{fin}; and (4) the V_{Tsat} variations for the large sizes of T_{fin} and H_{fin} are greater than that of the small sizes of T_{fin} and H_{fin}. This means that for the greater size of the same L_{gate}, the gate dominating capability over channel is more slightly. In the contrast, for the smaller size of FinFET, almost all the channel volume can be induced by the gate electrode bias. The effect that the punch-through current increases with the increase of the size of FinFET can be explained by the gate electrode controlling the channel volume incompletely. Thus, in order to achieve the desired threshold voltages will be a significant challenge in triple-gate devices. Threshold voltage control requires gate workfunction tuning, channel doping, or asymmetrical degigns [15-17].

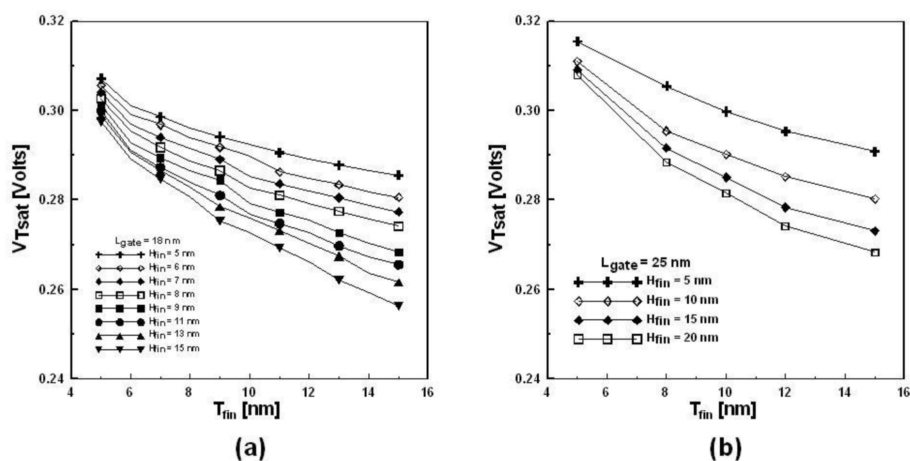

Fig. 5 The V_{Tsat} plot vs. (a)T_{fin} and H_{fin} under the fixed L_{gate} of 18 nm, (b) T_{fin} and H_{fin} under the fixed L_{gate} of 25 nm.

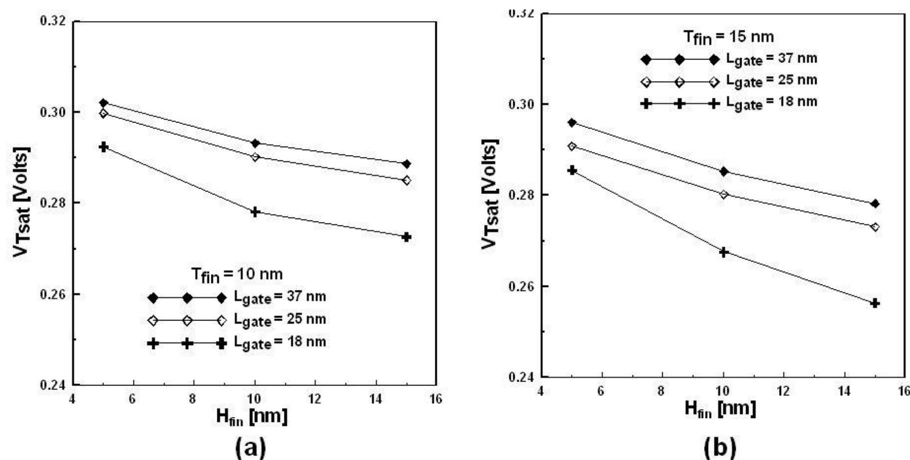

Fig.6 The V_{Tsat} plot vs. H_{fin} and L_{gate} under different T_{fin}: (a) T_{fin} is 5 nm, (b) T_{fin} is 15 nm.

If small channel length of planner MOSFET are not scaled properly and the source/drain junctions are too deep or channel doping are too low, there can be unintended electrostatic interactions between the source and drain known as Drain Induce Barrier Lowing. This leads to punch-through leakage or breakdown between the source and the drain, and loss of gate control. In deep-submicron era, the planner MOSFET can not suppress the punch-through effect. The FinFET gives the advantage to overcome this effect. Thus, to investigate further the DIBL effects of FinFET device, a data extraction of experimental results may be used in detail. Simplistically, the onset of DIBL is sometimes considered to correspond to the drain depletion region expanding and merging with the source depletion region, and causing punch-through breakdown between the source and drain. On the other hand, in order to increase the part of the channel doping concentration which are known to degrade the DIBL, but improve the drive current. Fig. 7 (a) shows the DIBL increase with T_{fin} and H_{fin}. Fig. 7(b) shows the increment of DIBL effect with variation of L_{gate} from 18 nm to 25 nm and that of L_{gate} variation from 25 nm to 37 nm. The later sample is approximate the twice times over the fomer sample. This result seems to represent the regulation, which is the DIBL increment from the divination of these two generations to next two generation with the same T_{fin} and H_{fin}.

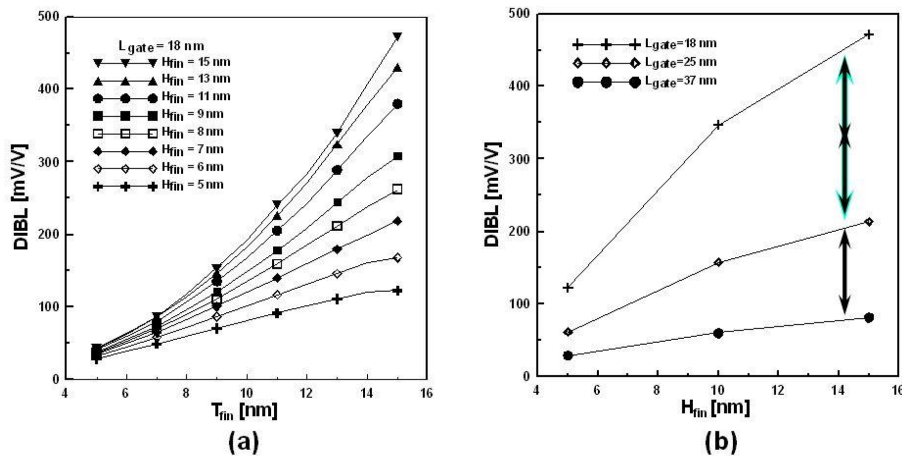

Fig. 7 (a) The DIBL plot vs. T_{fin} and H_{fin} under L_{gate} = 18 nm, (b) DIBL increment with the H_{fin} and different L_{gate}.

Fig. 8 shows the plots of on-to-off current ratio variations with H_{fin} and T_{fin} under the fixed L_{gate} of 18 nm. The on-to-off current ratio decreases with the T_{fin} and/or H_{fin} was exhibited. It can be also seen that the result of a proper submicron-gate bias not only greatly improves the on-state current, but also effectively reduces the off-state leakage. Extremely high on-to-off current ratio (up to $10^{5.3}$ times) could thus be achieved. The drain-to-source space region extends completely across the channel volume, also known as the punch-through of FinFET. In this situation, the barrier between the source and drain is

completely eliminated and a very large current would exist. Thus, for the deep-submicron device, the larger device dimension causes a larger off-leakage current.

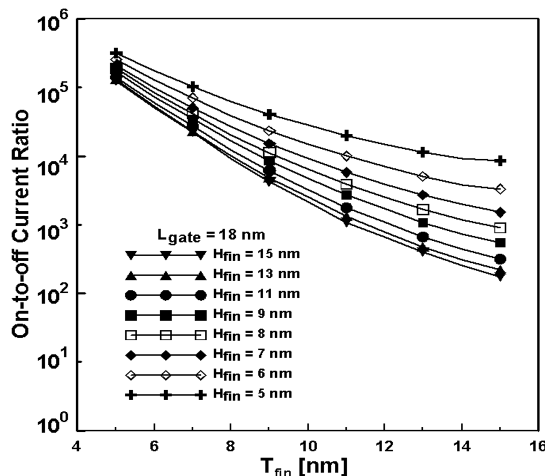

Fig. 8 The on-to-off current ratio vs. Tfin and Hfin under different Vd and Lgate = 18 nm: (a) Vd = 0.8 V (Vdd).

This effect is due to the punch-through of FinFET. To obtain high on-to-off current ratio, the size of the FinFETs should be made as small as possible. Essentially, carrier transport in reduced-sized FinFET would be very different from that of large sized devices. Phenomena that are negligible in large devices become limiting factors as device geometries are reduced.

Equation (1) can be used to find the subthreshold swing (SS), needed to reduce the current by one decade. By definition,

$$\mathrm{SS} = \mathrm{k} \times \left\{ \frac{\mathrm{d}[\log(\mathrm{I_d})]}{dV_g} \right\}^{-1} \qquad (1)$$

where $k = 1000$. The SS represents the capability of gate inducing the channel in a device. The lower of SS indicates the higher capability. Thus, the desired SS is defined below 100 mV/decade [18]. The SS variations was shown in Fig. 9. Fig. 9(a) exhibits the SS variations at V_d=0.05V. Fig. 9(b) presents the SS variations at V_d=0.8V.

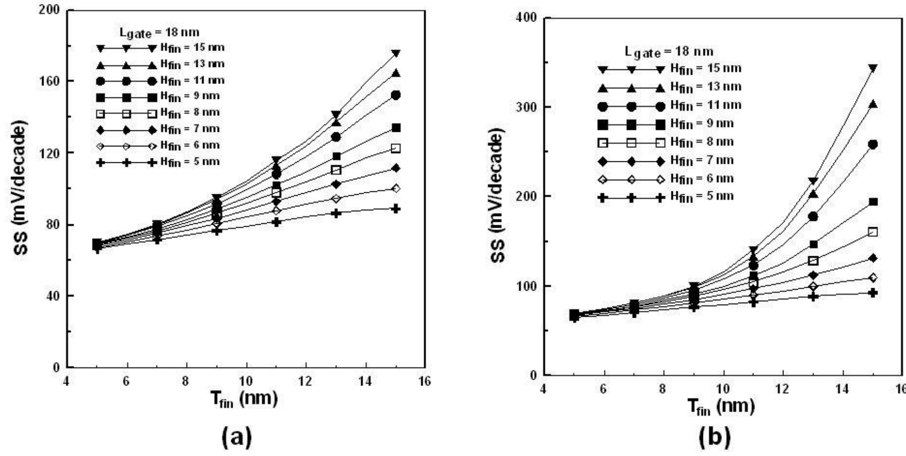

Fig. 9 The SS vs. Tfin and Hfin under the different Vd and Lgate = 18 nm:
(a) Vd = 0.05 V, (b) Vd = 0.8V (Vdd).

In these two figures, it can be seen that: (1) the SS increases with increasing T_{fin}; (2) the SS increases with increasing H_{fin}; (3) the SS variations of T_{fin} is more significant than that of H_{fin}; and (4) the SS variations for the large sizes of H_{fin} and T_{fin} are greater than that of the small sizes of H_{fin} and T_{fin}. For the H_{fin} sample, the most improvement is the reduction of the subthreshold swing, SS, from 67mV/decade at T_{fin}=5nm to 89 mV/decade at T_{fin}=15nm. Thus the improvement in the subthreshold swing at T_{fin}=5nm is about a factor of 1.3. Other improvements of subthreshold swing, SS, include higher carrier mobility, higher transconductance, higher threshold conductivity, lower power consumption, lower junction leakage current, and lower metal-line resistance.

Conclusions

Using 3-D numerical simulation and analytical modeling, the scaling effects from SCE in FinFET device design are presented. The studies in this paper also provide a tractable theoretical base for design space in FinFET. 3D simulation and device design of FinFET with channel length in the range of 37~18 nm has been presented. To determine the optimum SOI thickness of triple-gate FinFET, electronic characteristics are also investigated. Important results obtained form 3D simulation of FinFET are summarized as follows:

(1) V_{Tsat} decreases with increasing L_{gate} and decreases with the increase of T_{fin} and H_{fin}.

(2) The DIBL increases considerably with L_{gate} especially for large-sized devices. For DIBL<100, it requires $T_{fin} \le$ 7nm @ L_{gate} = 18nm, or $T_{fin} \le$ 8nm @ L_{gate} = 25nm, or $T_{fin} \le$ 10nm @ L_{gate} = 37nm.

(3) The optimal structure for SS<100: $T_{fin} \le$ 9nm @ L_{gate} = 18nm, or $T_{fin} \le$ 12nm @ L_{gate} = 25nm, or $T_{fin} \le$ 15nm @ L_{gate} = 37nm.

The on-to-off current ratio could be enhanced by decreasing either T_{fin} or H_{fin}. Effect of T_{fin} on the on-to-off current ratio is seen much stronger than that of H_{fin}.

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