

# The Study of N-SiCN/P-PS Junction for Low Cost and High Temperature Ultraviolet Light Detecting Applications

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## Abstract

In this work, we report a comparative study of both lateral n-SiCN/p-porous silicon and vertical n-SiCN/p-porous silicon heterojunctions for low cost and high temperature ultraviolet (UV) detecting applications. The porous silicon (PS) layer has the features of high resistivity and the flexibility, thus suppresses the dark current of the optical sensing device at high temperature. The cubic crystalline n-SiCN films were deposited on p-(100) PS substrate with rapid thermal chemical vapor deposition (RTCVD). In room temperature, the measured photo/dark current ratio of the lateral n-SiCN/p-PS and vertical n-SiCN/p-PS heterojunctions with and without irradiation of 254 nm UV light, under  $-5$  V bias and  $0.5$  mW/cm<sup>2</sup> are 98.2 and 84.6, respectively. The ratios are decreased to 17.6 and 14.1 at 150 °C, respectively. The results are better than that of reported SiCN or  $\beta$ -SiC UV detector on Si substrate without porous treatment.

**Keywords** : heterojunction, ultraviolet (UV), porous silicon (PS), SiCN, RTCVD.

## 1. Introduction

Ultraviolet (UV) photodetectors have many potential applications such as solar astronomy, missile plume detection, combustion process monitoring, biological, and chemical applications [1], thus has drawn much attention in the recent years. In the past, major compact UV sensors were developed with GaN,  $\beta$ -SiC on Si, 4H-SiC, and 6H-SiC. The GaN or 6H-SiC UV sensor has better high temperature characteristics [2], [3], but is more expensive [4], [5]. Even, the  $\beta$ -SiC on Si substrate is low cost, and has been studied widely. Nevertheless, its photocurrent/dark current ratio (PDCR) is low, especially in high temperature. Therefore, it is interesting to search a new material for low cost and high temperature UV detecting applications. It has been reported that the cubic crystalline SiCN (c-SiCN) film deposited on p-Si(100) substrate by the rapid thermal chemical vapor deposition (RTCVD) has wide band gap of  $3.2 \sim 4.4$  eV [6], which is larger than or comparable to 6H-SiC of 3.0 eV,  $\beta$ -SiC on Si of 2.2 eV, GaAs of 1.42 eV, and GaN of 3.36 eV [4]. Besides, the epitaxial SiCN on Si substrate offers the advantages of economic Si material and very large scale integrated (VLSI) compatible processing thus



lowering the cost to enhance the applications. On the other hand, the porous structure features high resistivity and the flexibility to relax the stress caused by the different thermal expansion coefficient between different materials, thus suppresses defect generation in the interface, and reduction of dark current at high temperature [7], [8]. Hence, the c-SiCN deposited by RTCVD on porous Si (PS) substrate is employed to construct c-SiCN/PS heterojunction for the low cost UV detecting application.

In this work, two structures i.e., lateral n-SiCN/p-PS and vertical n-SiCN/p-PS heterojunction were developed for comparative study. The PDCR of both structures under 254 nm wavelength light source at various operating temperatures were measured and compared. The lateral n-SiCN/p-PS heterojunction has the better PDCR in both room and high temperatures than the vertical heterojunction.

## 2. Experiments

Figures 1(a) and (b) illustrate the structure diagrams of the lateral n-SiCN/p-porous silicon and vertical n-SiCN/p-porous silicon devices, respectively. In preparing the devices, the electrochemical anodization method was used to form the PS layer on (100) p-type Si substrate with resistivity of 4 ~ 10  $\Omega$ -cm [9], [10]. Prior to the anodization, Al (3000-5000 Å) film was deposited on the back side of the sample and annealed with 450 °C for 15 minutes in forming gas to distribute the etching current uniformly. The anodic etching was carried out in an HF-ethanol solution (HF: H<sub>2</sub>O: C<sub>2</sub>H<sub>5</sub>OH=1: 2: 2), at a constant current density of 30 mA/cm<sup>2</sup> for 10 minutes to get a PS layer with thickness 0.8 to 1.2  $\mu$ m [7], [8]. The junction area is 0.8 × 0.8 cm<sup>2</sup> for both structures. To prepare the lateral n-SiCN/p-PS heterojunctions, the p-PS/Si substrate after cleaning was sent to chamber of a rapid thermal chemical vapor deposition (RTCVD), then rapidly raised the substrate temperature to 1150 °C and held for 15 minutes to deposit the 6000 Å thick photosensitive n-SiCN film. Sequentially, the Ni (1500 Å) and Al (3000 ~ 5000 Å) metals were evaporated on n-SiCN surface and p-PS surface to form the top finger electrode, respectively. Finally, the samples were annealed at 450 °C for 15 minutes to form the ohmic contact. The flow rates of SiH<sub>4</sub> (reaction gas), C<sub>3</sub>H<sub>8</sub> (carbon source), NH<sub>3</sub> (reaction gas), PH<sub>3</sub> (doping gas), are 80 sccm, 80 sccm, 80 sccm, 10 sccm, respectively. The growth rate is about 400 Å/min. The same processes were also applied to complete the vertical n-SiCN/p-PS heterojunction (Figure 1(a)), except Al now is deposited on the back of Si substrate to as another terminal contact. A more detailed description for growing c-SiCN and subsequent material characterizations can be found in elsewhere [11].

## 3. Results and discussion

The result of the pore electrochemical anodization procedure was investigated to study the microstructure of the porous silicon (PS) surface layer by means of scanning



electron microscopy (SEM), and shown in Figures 2a, and 2b for the top PS surface on the Si substrate and the side view of a cleaved section, respectively. As seen, the porous rod is column like with depth and diameter void about  $0.8 \sim 1.2 \mu\text{m}$ , and  $250 \sim 350 \text{ nm}$ , respectively. Figure 3 shows the spectral responsivity measurement for n-SiCN/p-PS/p-Si heterojunction under the room temperature. The peak value is around 260 nm, which implies both structures are preferred for deep UV detecting applications. Figures 4, 5 and 6 show the dark currents, photocurrents, and PDCR measured under reversed bias and various temperatures with a HP4145B semiconductor parameter analyzer for both heterojunctions, respectively. The photocurrents were measured under the irradiation of 254 nm UV light source (Model: UVP, UVGL-58) with  $0.5 \text{ mW/cm}^2$  power [4]. The PDCR is defined as  $\text{PDCR} = (I_p - I_d)/I_d$ , where  $I_d$  is the dark current;  $I_p$  is the photocurrent (i.e. the current under illumination). The photocurrents/dark currents of vertical n-SiCN/p-PS and lateral n-SiCN/p-PS heterojunctions at room temperature, under  $-5$  volts bias are  $1.01 \times 10^{-5} \text{ mA}/1.18 \times 10^{-7} \text{ mA}$ , and  $3.96 \times 10^{-6} \text{ mA}/3.99 \times 10^{-8} \text{ mA}$ , respectively. However, as the temperature is raised to  $150 \text{ }^\circ\text{C}$ , the dark currents are raised to  $7.41 \times 10^{-6} \text{ mA}$  and  $3.33 \times 10^{-6} \text{ mA}$  for vertical junction and lateral junction, respectively. In other words, at room temperature and high temperature, the PDCR for lateral/vertical heterojunctions are 98.2/84.6, and 17.6/14.1, respectively. These results are better than the reported  $\sim 5.4$  in MSM (metal-semiconductor-metal) structure [12] or  $\sim 60$  in P-I-N (p-type/intrinsic/n-type) structure of  $\beta$ -SiC [8] on Si substrate UV detectors under room temperature. We attribute the improvement in the PDCR of this work to the reduction of dark current by the addition of the PS layer. As shown in Figures 1(a) and 1(b), the high resistivity ( $\sim 3 \times 10^7 \Omega\text{-cm}$ ) of the layer offers a high resistance (about  $3 \text{ k}\Omega$  for the vertical junction, and  $6 \text{ k}\Omega$  for the lateral one) to retard the dark current. Besides, the PS layer is flexible thus relaxing the stress caused by the different thermal expansion coefficient between the n-SiCN and the p-Si substrate. Consequently, the generation of defects in the interface is also suppressed. The larger quantity of defects in the interface will become as the traps to assistance the tunneling of electron and hole through the band gap, thus results in higher leakage current (dark current) and lower PDCR. Furthermore, a slightly higher PDCR is found for the lateral junction both in room temperature and  $150 \text{ }^\circ\text{C}$ . We suspect one of the most possible reasons for the tiny differences in PDCR is that the lateral junction has a resistances across both the PS layer and the Si substrate (as shown Figure 1) larger than that of the vertical junction, thus results in a lower field across the n-SiCN/p-PS region, and in turn the less dark current. However, under the dark current of  $1.18 \times 10^{-7} \text{ mA}$ , only results mV for  $3 \sim 6$  kilo-ohms, hence another factors such as uniformities of PS and c-Si, and experiment accuracy will also influence the PDCR, thus should be studied more in future.

Furthermore, Figure 7 shows the low angle X-ray diffraction (XRD) spectra of the n-SiCN/p-PS junction. Because of the hetero-epitaxial growth of SiCN film on the p-PS



layer, both diffraction patterns of crystalline Si (c-Si) and crystalline SiCN (c-SiCN) are superimposed, thus, leads to the n-SiCN/p-PS layer has an obvious peak located at the diffraction angle  $46.06^\circ$  [13], and one peak at  $69.07^\circ$  for Si substrate [14]. The FWHM (full width at half maximum) of the SiCN peak at  $46.06^\circ$  is  $2.8^\circ$ , which is a little higher than 1.01 for c-SiCN on the Si substrate. It is well known, the FWHM is related to the crystalline of the film, and hence the higher value in FWHM means the porous Si substrate degrades the crystalline of SiCN. This is supported from the examination of morphology the n-SiCN film deposited on p-PS with SEM and AFM (atomic force microscopy) as shown in Fig. 8 and the insert, respectively. The SEM photo shows the surface is not very smooth. In addition, based on AFM measurement, the roughness/root mean square (RMS) for the device is 7.529 nm/9.628 nm, which is larger than the 2.654 nm/3.372 nm for the c-SiCN on Si. Therefore, we conclude that the porosity of the Si substrate should be compromised between the high resistivity and the influence on the deposited SiCN film quality. We find that the PDCR of the developed devices can be improved if the porosity of the Si substrate is optimized.

#### 4. Summary

Both of lateral n-c-SiCN/p-PS and vertical n-c-SiCN/p-PS heterojunctions have been investigated and compared for low cost and high temperature ultraviolet (UV) detecting applications. The cubic c-SiCN films were deposited on p-PS with RTCVD. At room temperature, the PDCR for lateral heterojunction and vertical heterojunction are 98.2, and 84.6, under  $-5$  V bias, with and without irradiation of 254 nm UV light with power of  $0.5$  mW/cm<sup>2</sup>, respectively. Even the temperature is raised to  $150^\circ\text{C}$ , the PDCR are still attained to 17.6 and 14.1, respectively. Compared to the reported UV detectors with SiCN or  $\beta$ -SiC deposited on conventional Si, the developed lateral n-SiCN/p-PS heterojunction has the better current ratio both in room and high temperature, thus has higher application potential for high temperature UV sensors.

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### Figure Caption

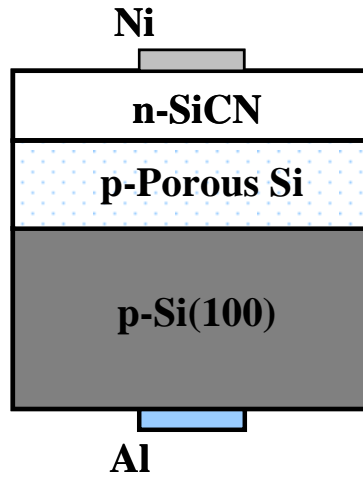
- Fig.1** Schematic cross section of n-SiCN/p-PS junctions for (a) vertical structure, (b) lateral structure.
- Fig.2** SEM photos of the PS layer on Si Substrate for (a) top view and (b) cross section side view.
- Fig.3** The typical responsivity of the n-SiCN/p-PS/p-Si heterojunction.
- Fig.4** The dark current (a), and photocurrent (b) for the vertical n-SiCN/p-PS heterojunction.
- Fig.5** The photocurrent (a), and dark current (b) for the lateral n-SiCN/ p-PS heterojunction.
- Fig.6** PDCR as a function of measuring temperature for both vertical and lateral



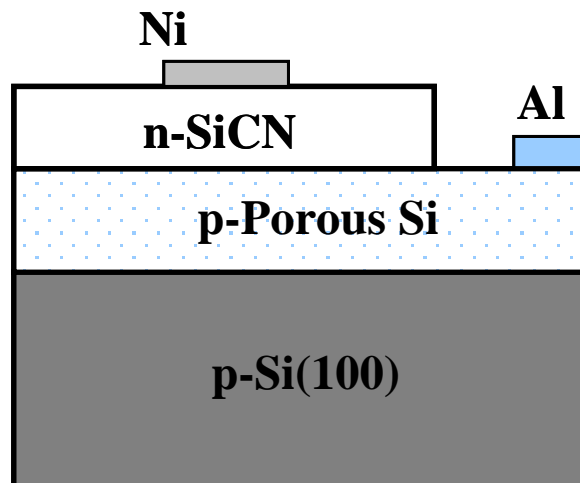
n-SiCN/p-PS junctions.

**Fig.7** XRD spectra of the n-SiCN film deposited on p-PS layer.

**Fig.8** SEM photo and AFM photo (insert) of the n-SiCN film deposited on p-PS layer.

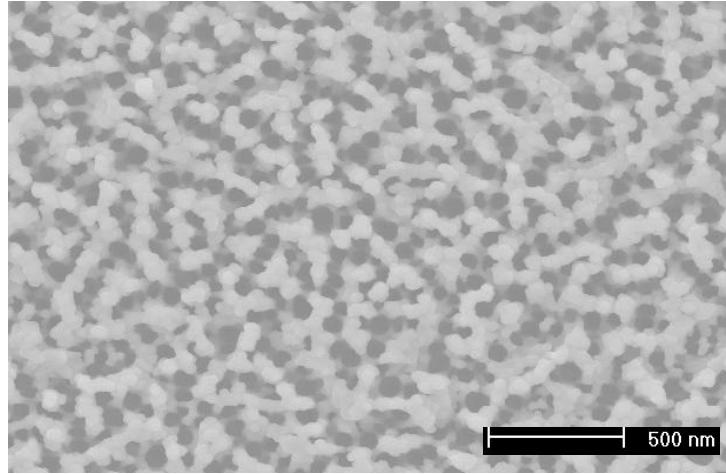


**Fig. 1(a)**

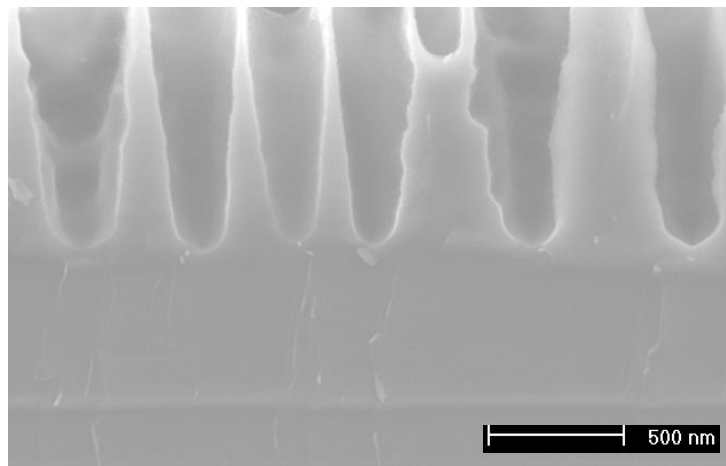


**Fig. 1(b)**





**Fig. 2(a)**



**Fig. 2(b)**



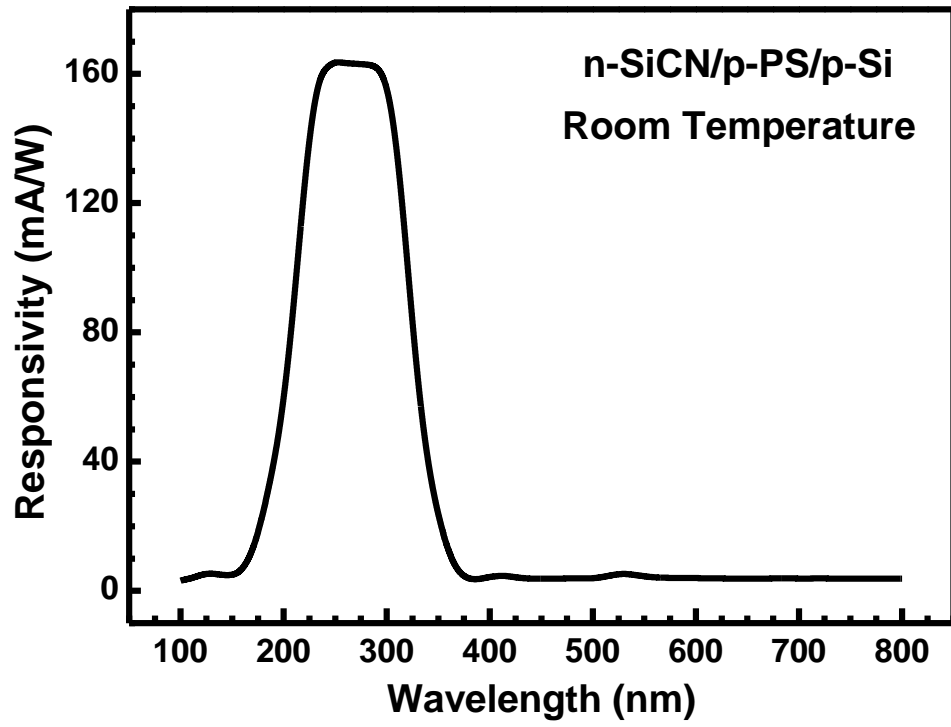


Fig. 3





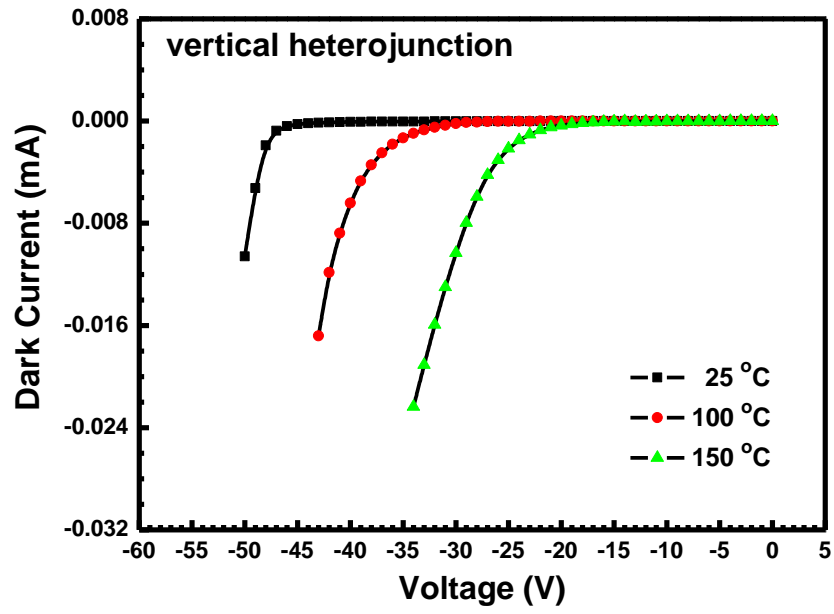


Fig. 4(a)

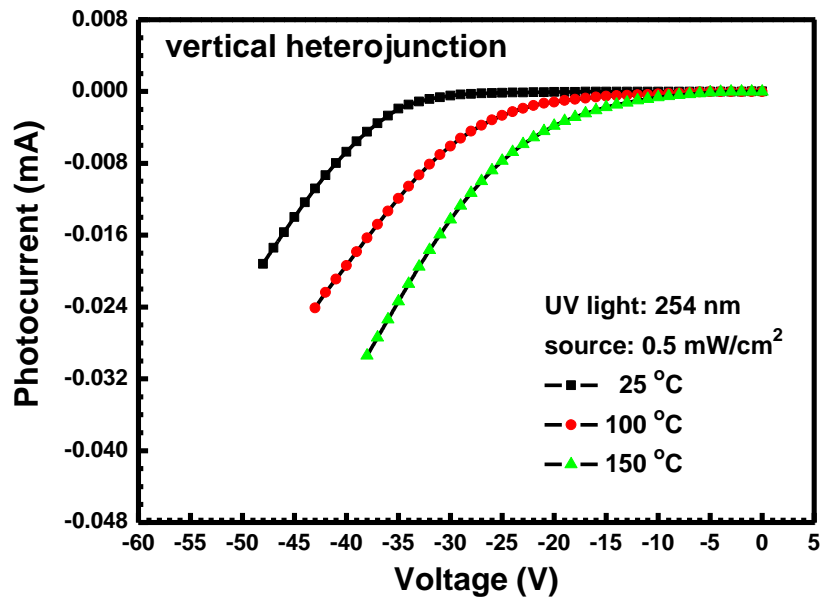


Fig. 4(b)



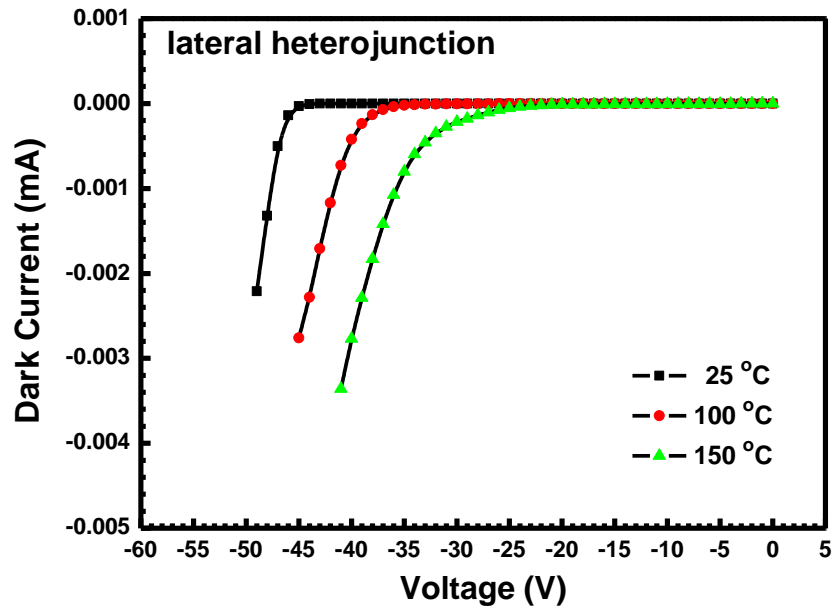


Fig. 5(a)

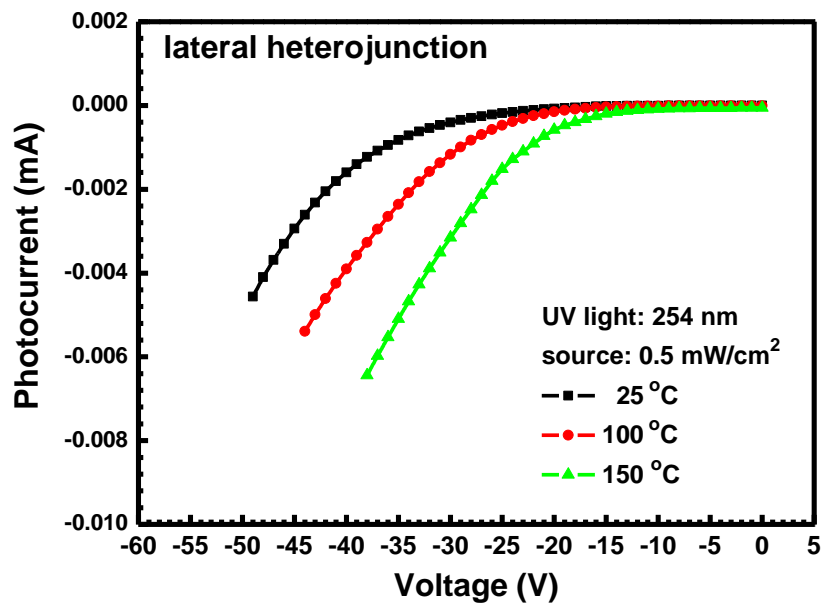


Fig. 5(b)



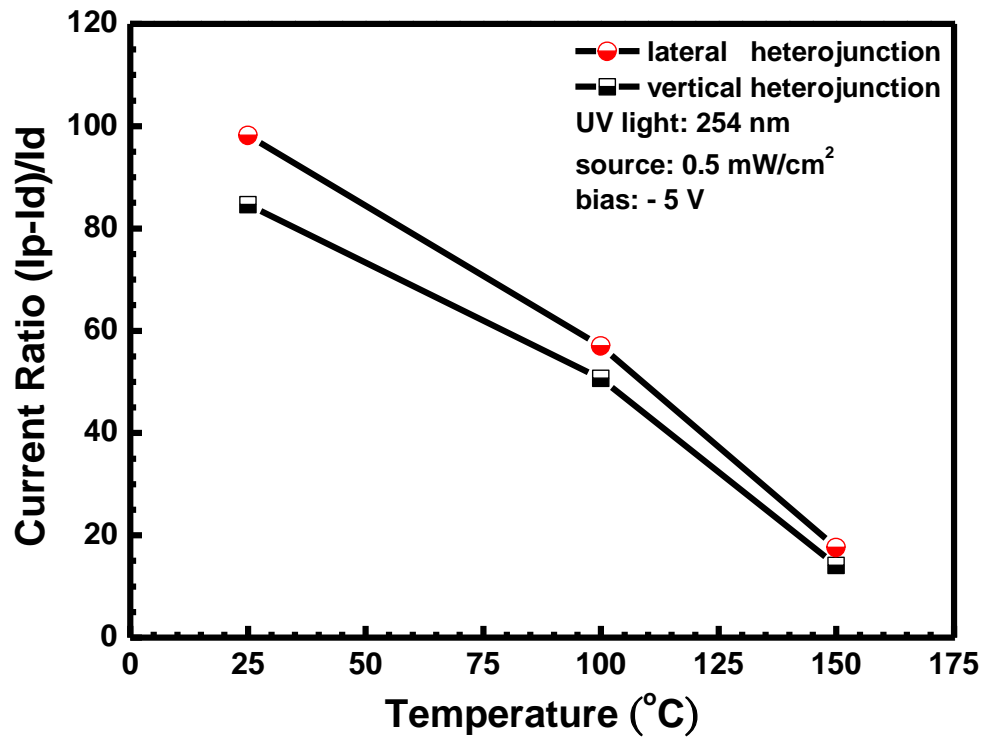


Fig. 6



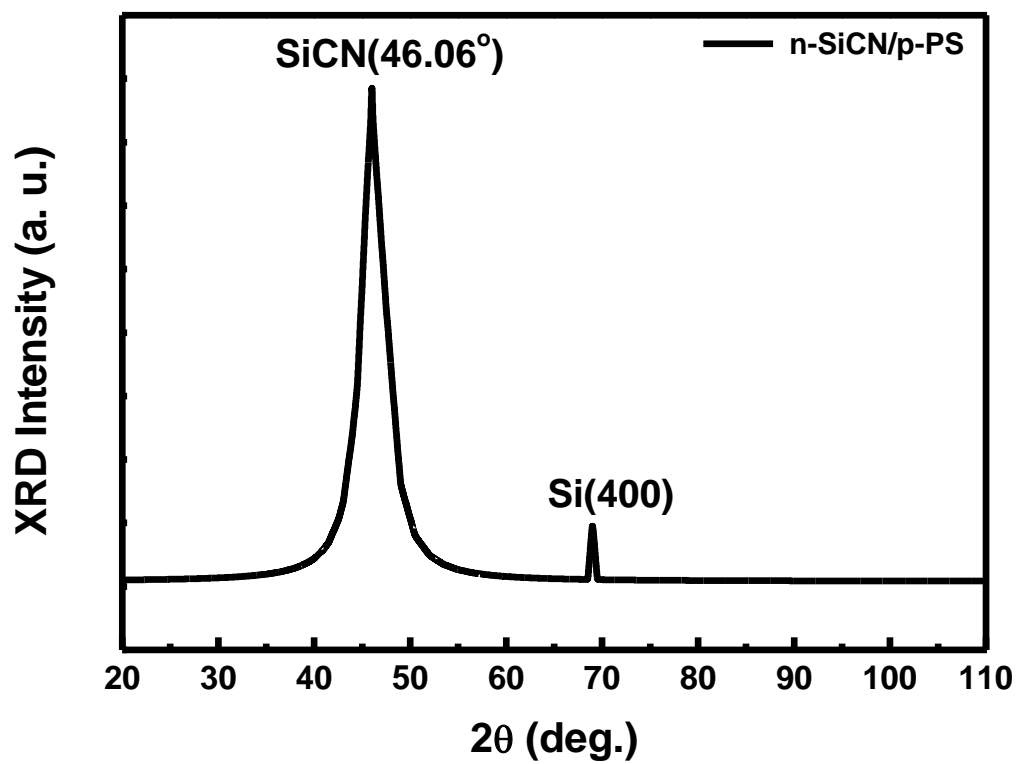
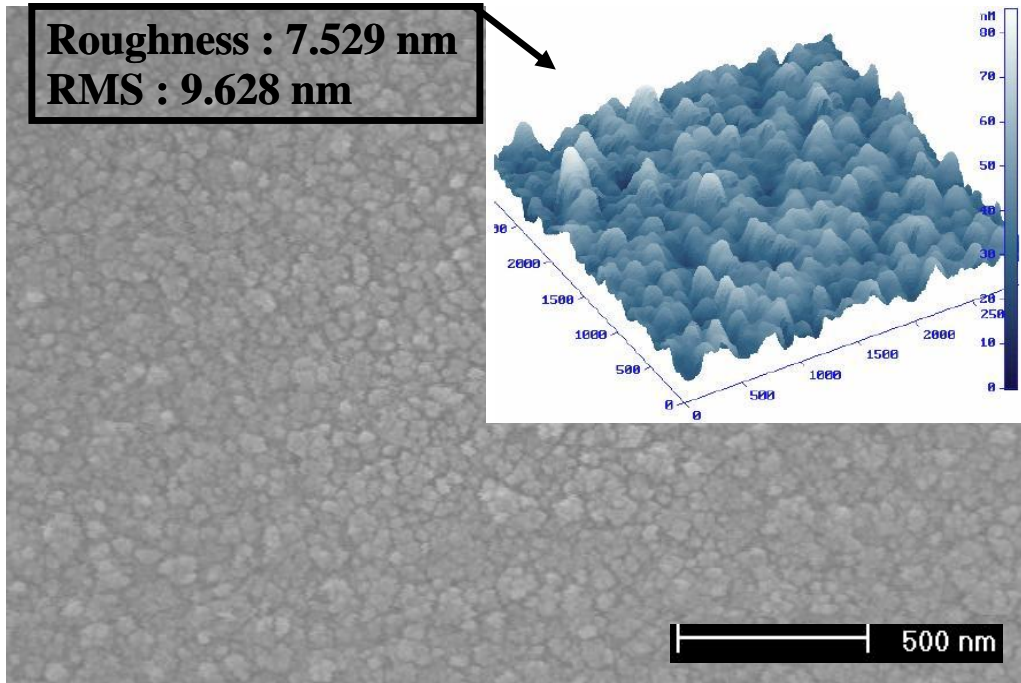


Fig. 7





**Fig. 8**

